A THESIS

FOR THE DEGREE OF MASTER OF SCIENCE

All Printed Resistive Switching Memory Devices Based on Solution Processed Materials for Wearable Electronics

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November 2018

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A thesis submitted in partial fulfillment of the requirement for the degree of Master

2018. 11

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Dedicated to my beloved family without whom I would not be where I am today and to my dear Father & Grandfather.

“Life consists of two days, one for you one against you. So when it's for you don't be proud or reckless, and when it's against you be patient, for both days are test for you.”

Hazrat Imam Ali Ibn Abu-Talib A.S

Acknowledgements

In the name of ALLAH, the Most Gracious, the Most Merciful. All praise to Almighty Allah for blessing me with strength, courage, and knowledge; and helping me out constantly to achieve this honor. He has never left me helpless and has always guided me in the right direction throughout this long journey. Without His help and blessings, I would not have been able to complete a single step. I pray to Him to make the path of my future easy and help me in doing something good for humanity.

My sincerest gratitude is towards my parents, brother and sisters, who have always supported me at all steps of my life. They have provided me with everything in their power and beyond. Without their love and constant support, this journey would have ended far earlier for me. It was their encouragement and motivation that kept me going and I am indebted to them forever. They have always inspired me to become a better human being and put others before myself. I would also like to thank my sisters.

The day I joined Department of Ocean System Engineering (OSE), I was nothing but now the day I am leaving, I am feeling that I learnt a lot during my stay to start my career in research and technology and can use my potential for the wellbeing of humanity. This is all about the training of Prof. Jinho Bae who polished my skills with novel ideas and ground-breaking thoughts. I would like to pay my heartiest thanks with best regards to Prof. Jinho Bae, who put his full efforts to give me confidence, access over all the resources in the laboratory and hire external resources as well to accomplish the task. During my M.S studies, Prof. Bae provided me shelter against all kind of crisis from morally depraved conditions to financial problems.

I am especially grateful to Shawkat Ali who introduced me to my supervisor Prof. Jinho Bae for M.S studies at OISE Lab, Jeju National University. I would like to thanks my colleagues in OSE Lab and friends in the Jeju University as well. Few of the names are coming in my mind including Dr. Gul Hassan, Dr. Shawkat Ali, Dr. Arshad Hassan, , Muhammad Asim Raza, Jung-Min Kim, Hina Ashraf, Sehrish

Malik, Wafa Shafqat, Dr. Memom Sajid, Dr. Irshad, Yuhan Choi, Dr. Afaq, Dr. Muqeet, Dr. Waqar, Dr. Siddiqui, Dr. Afaq Muhammad, Afaque Maznzoor soomro, Faiza Jabbar, Shahbaz Raza, Adeel Rafiq, Adeel Farooq, Mutee, Asad, Muhsin, Imran, Fiza, Iqra, Jahanzib, Israr, Shabeer, Asif, Tahir, Ali, Faisal, Sajad, Zeshan, Tahseen Elahi Chattha, Muzahir and many more.

I would love to present my tribute to my Grandfather, Father, loving Mother, Sisters, and Brother (Dost Muhammad, Jahanzeb Khan, Dilshad bibi, Shaista Jahanzeb, Sidra Shahzad, Saadia Nabeel and Muhammad Uzair Khan, Dost Muhammad). All of my family has always been a source of appreciation and admiration throughout my life either in my professional career or student life. I would like to disclose that Almighty Allah bestowed me such a noble and dominating Figures in my life, without whom I could not have predicted myself to accomplish this task.

In the end, I would like to acknowledge and promise myself to be bind by the golden tips of life as positive thinking, hard work and consistency in execution of the idea.

Muhammad Umair khan

Abbreviations

DMF	N,N-dimethyl-formamide
FESEM	Field Emission Scanning Electron Microscope
HRS	High Resistance State
ITO	Indium Tin Oxide
I-V	Current-Voltage
LRS	Low Resistance State
Memristor	Memory Resistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PET	Polyethylene terephthalate
PVP	Poly(4-vinylphenol)
TPD	N, N′-Bis (3-methylphenyl)-N, N′-diphenylbenzidine
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene)poly(styrenesulfonate)
ReRAM	Resistive Random Access Memory
SCLC	Space Charge Limited Current
TCLC	Trap Charge Limited Current
ZrO_2	Zirconium Dioxide
R_{OFF}	High Resistance State
R_{ON}	Low Resistance State
PVOH	Poly (vinyl alcohol)
ZnO	Zinc Oxide

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Abstract

In recent, wearable and printed memory devices have got tremendous attention because it is highly desirable for the next-generation technologies and customized applications. Printed electronics have the potential to revolutionize the spread of electronic applications and can be easily interfaced with human machine interface devices and systems. In this thesis, we address the solution processed based flexible printed resistive memory devices through a spin coating technology. These devices can be mounted on any desire surface. To realize these devices, we utilize a spin coating technology to fabricate memory device on ITO coated flexible PET substrate.

To summarize, we fabricated three printed resistive switching devices using PEDOT: PSS, ZnO, PVP, ZrO_2, TPD and PVOH. We also optimized the memristor design and materials for high R_{OFF}/R_{ON} ratio, long retention time, high stability and endurance cycles. We also investigated different memristor mechanisms to support its performance. Different structures were investigated based on heterojunction and composite of two different materials to optimize following parameters like device stability, memory device with high charge density and to control the sneak current problem in cross bar array of memory devices as given in section 2.2, 2.3 and 2.4.

In section 2.2, initially we propose a stable non-volatile resistive switching based on nano-composite of inorganic and organic materials, Zirconium dioxide (ZrO_2) and Poly (4-vinylphenol) (PVP), respectively. We improved the stability of the memory device by mixing different blending ratios of PVP with ZrO_2 and we achieved a stable memory function. The novel heterojunction junction memory device is proposed in section 2.3, which is based on N,N′-Bis (3-methylphenyl)-N,N′-diphenylbenzidine (TPD) and Poly(3,4-ethylenedioxythiophene)-

poly(styrenesulfonate)/ Poly(vinyl alcohol) (PEDOT:PSS/PVOH) composite. This memory device is highly stable and at some instant and we reduced the sneak current in negative axis. In order to completely block sneak current in memory device and to realize an asymmetric function, we propose a novel schottky diode resistive switching device based on zinc oxide (ZnO) and poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) heterojunction in section 2.4.

For high density integrations of nonvolatile memory devices, crossbar arrays with single bit memristor cells are demonstrated. However, those crossbar designs incur severe sneak currents problems, which are resulted in high read/write error and large power consumption during the individual cell access. In a passive crossbar resistive array, each row-column pair is connected by a resistor that can be either in the HRS or the LRS corresponding to the logic value stored in the cell. The sneak path problem occurs when a memory cell in the HRS is being read, while a series of cells exist in parallel to it, if the neighboring cells are in LRS the sneak current issue is more exacerbated thereby causing it to be erroneously read. The sneak currents not only make the data erroneous but also dissipate extra power because the currents are flown through the neighbor memristors and added to the element current at the same terminal. Especially, in large size arrays, the sneak currents problem becomes more pronounced, thus individual bits cannot be explicitly accessed. As techniques to overcome the sneak currents problem, a set of different approaches have been reported in the literature including a rectifying element connected to a memristor in series at each cross-point and anti-serial memristors complementary resistive switches. All these attempts would minimize the sneak currents, but until now the sneak current problem in a passive crossbar array has not been addressed

satisfactorily. So this research opens a way to next-generation printed and flexible resistive switching devices and its customized applications. Hence, the proposed schottky diode based memory device can be applied in flexible resistive switching devices to blocking sneak current problem. The fabricated resistive switching devices were tested for their electrical, optical, chemical, structural and mechanical behavior to conform and verify the solution processed based device fabrication approach.

Chapter 1 Introduction

1.1 Solution Processed Printed Electronics

Solution processed printed electronics is a new stem of electronics engineering where printable and functional materials are directly fabricated through printing technologies on desire substrates to make customized electronic devices and systems. Printable electronics is quickly grooming because of its plenty advantages over conventional rigid type electronics such as Silicon or Gallium Arsenide, which are fabricated in clean-room environments and complicated processes. Rigid type electronics have the limitation and can't be used or satisfy the growing demands forced by new applications such as mechanical flexible or compatible with biological systems. To full-fill these missing gapes, printed electronics plays an important role with more energetic style including low temperature, easy to fabricate, environmental friendly, low cost and ambient conditions processing. Both organic and non-organic materials are used for printed electronics as substrates or active layers. But printed organic electronics have attracted more attention as some of the printed organic electronic devices have already commercialized in electronics market for large-area applications such as, organic thin film transistors (OTFTs) or especially organic LEDs (OLEDs) and they are already used in modern displays and TVs. In the organic electronics, mostly the polymers are used for substrate as well as active layer. Using polymers substrates for electronic systems is opening new gateway in the field of micro engineering. Polymers materials have the potential of making electronics environmental friendly, disposable, biocompatible or biodegradable and very low-cost. Some of the polymers are stretch or deform into subjective shapes without losing their properties. Some of the applications of printed

electronics are shown in Figure 1.1 Printed electronics is further divided into flexible and stretchable electronics based on the materials and its nature.

1.2 Flexible Printed Electronics

Flexible printed electronics market is fastly growing as they can be used in thousands of customized flexible application and systems Mostly the flexible electronics can be wearing and are used for day-to-day application such as flexible sensors for human motion detection, flexible electrodes and displays, and for biological applications. For the realization of flexible electronic devices, mostly flexible substrates are used such as PET, PDMS, polyurethane and flexible bio substrates Etc. Printed stretchable electronics are also called elastic electronics. It is the technology of depositing stretchable electronic devices onto a stretchable substrate or embedded them entirely in the stretchable materials such as PDMS, Polyurethane and many others. In such stretchable electronics, mostly the polymers are utilized because of its long chain structure and stretchable properties.

Stretchable electronics is now considered as the branch of electronics which is sometimes called elastronics that is, a new emerging class of electronics. Stretchable electronics are expected to enable a new gateway towards customized electronic applications such as human skin, sensors for monitoring real time deformations, biological applications, stretchable energy storage devices and many more.

1.3 Technologies Utilized for Printed Electronics

In recent years there is a great progress in the field of printed electronics because of their environment-friendly, light weight, ease of fabrication, low-cost manufacturing and the availability of inexpensive substrates such as plastics, papers and textiles,

which formulate flexible electronics an eye-catching candidate for the next generation of customized electronics.

To fabricate the printed electronic devices and system, different variety of fabrication technologies are available in which some are commercialized whereas some of them are still under research. Main concern of the printed electronics technologies is to fabricate the functional materials on a desire substrate with precision, high accuracy and maintaining the uniformity and thickness of the thin film. Different printing technologies are used, including chemical bath, spin-coating, dip coating, doctor blade, metering rod, slot casting, spray coating, screen printing, inkjet printing and aerosol jet. All fabrication techniques have their disadvantages and advantages, some of them need vacuum chambers or special environment to process the fabrication of a device. Fabrication techniques are adopted according to materials because different materials require different environment such as specific temperature, pressure, humidity, light and vacuum. In this thesis, spin coating is used for the fabrication of devices

Spin coating has been used for several decades for the fabrication of thin films. A typical process involves depositing a small puddle of a fluid resin onto the center of a substrate and then spinning the substrate at high speed (typically measured in revolution per minute rpm). Centripetal acceleration will cause the resin to spread to, and eventually off, the edge of the substrate leaving a thin film of resin on the surface. Final film thickness and other properties will depend on the nature of the resin such as, viscosity, drying rate, percent solids, surface tension, etc. and the parameters chosen for the spin process. Factors such as final rotational speed, acceleration, and fume exhaust contribute to how the properties of coated films are defined. Schematic

diagram of a spin coater along with main components is shown in Figure 1.5a and a very simple process of spin coating flow chart is shown in Figure 1.5b.

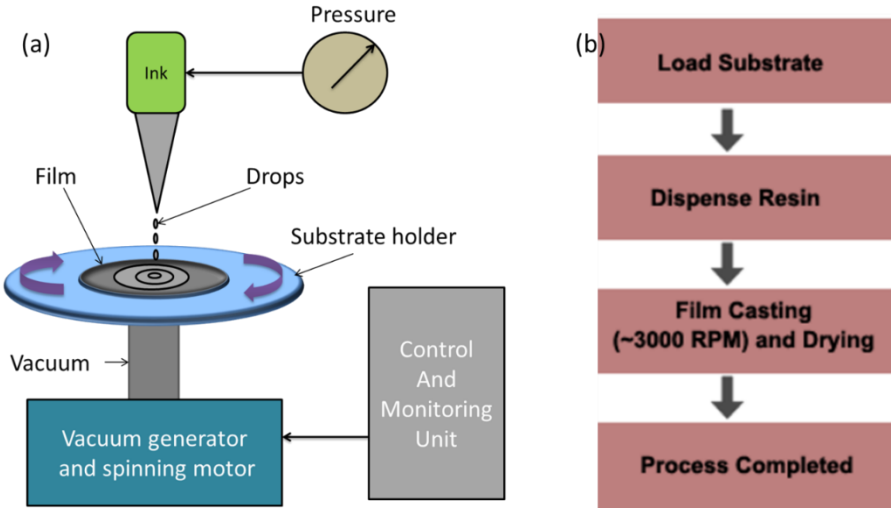

Figure 1.1 (a) Spin coater schematic diagram. (b) Simple spin coating process.

1.4 Objective of the Thesis

Printed electronics is new emerging field that allow lost cost, large area, flexible and environmentally friendly applications. Some devices are matured and already have been used in electronic applications such as OLED display, RFID tags and humidity sensors etc. Since printed electronics is new field there is big room yet in the advancement of the printed electronics. Among the recent challenges of the printed electronics are: the fabrications techniques, encapsulation and reliable materials. The main objective of thesis is to address these challenges by exploring new functional materials to fabricate the resistive memory devices. Organic and inorganic materials are synthesized to make them printable with different printed techniques that enable large area fabrication. Spin coating is used for the fabrication of resistive devices, which is low cost and required ambient condition. The optical, chemical, mechanical

and electrical characteristics and statistical analysis has been carried out to make sure the reliability and direct printability of the electronic devices.

1.4.1 Outline of thesis

Chapter 2 deals with the memristor working, fabrication and characterization of Heterojunction based and composite based resistive memory devices. These devices are fabricated with spin coater technique. Resistive switching properties and resistive switching mechanism are investigated in the fabricated devices. This chapter also describes the fabrication of flexible resistive switches.

Chapter 2 Memristors

2.1 History and background

2.1.1 Memristor

In the conventional electronics, there are only three fundamental two-terminal passive circuit elements named resistor, inductor and capacitor. Based on simple symmetry arguments Leon Chua claimed that a fourth fundamental two-terminal passive circuit element is necessary to complement the other three. More specifically, Chua realized that out of the six possible pair wise combinations between the four fundamental circuit variables, namely, the current, voltage, charge, and flux-linkage, only five had been identified. He therefore postulated mathematically the memristor as the element relating the charge and the flux-linkage in order to establish the missing link as shown in Figure 2.1. In 2008, HP lab demonstrated the first physical memristor based on resistive switching in doped TiO_2. In 2010 Chua confirmed that every resistive switching device is a memristor. Memristor can be switched between two resistive states, low resistance state (LRS) and high resistance state (HRS) through external voltage bias. This particular feature makes it a transistor less switch that can be fabricated in very small size. Since that, it researched widely in the electronics field for the future non-volatile memory applications.

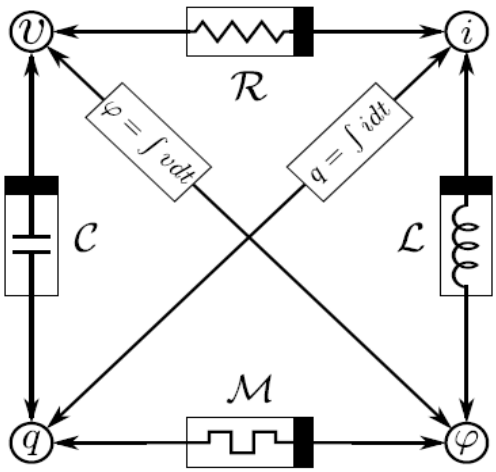

Figure 2.1 The diagram shows the six possible binary relations between the four fundamental circuit elements.

Resistive crossbar passive memories (ReRAMs) based on resistive switching is considered the next generation non-volatile memory (NVM) because of its ample advantages over the flash memory. As CMOS technology is reaching its limits in sense of materials, device size, fabrication plants and economics, ReRAM is the only hope to counteract the upfront challenges to the electronic industry. Resistive switches (transistor less) considered as a justified replacement for the memory devices and electrical switching elements have been researched productively for many. Solid electrolyte sandwiched between two metallic electrodes is considered to elucidate the reversible resistive switching characteristics. The sandwiched structures exhibit at least two distinct states when are being forced with opposite polarity. The change in the resistance is then exploited for the electrical switching and memory applications. The resistive switching devices are fabricated by simply sandwiching some metal oxide, polymer-based material, perovskite material, or even a vacuum nano-gap etc between two conducting electrodes. The resistive switch provides great data storage density due to its simple device structure. The sandwiched type structures are more reliable because these devices are resistance based so they keep their state unchanged even when the power absence.

2.1.2 Types of Memristors

As described in the previous section that as compare to an ordinary electrical resistor, memristor can be programmed or switched in different resistive states based upon the history of the voltage signal applied to the device. This phenomenon can be understood in a current-voltage (I-V) curve. Resistive switching are categories into two main types based upon the voltage polarity needed to the device operation.

2.1.2.1 Unipolar Memristors

If switching of the resistive switch is independent of the polarity of the voltage/current source and is dependent on the amplitude of the voltage/current then the switching is categorized as unipolar resistive switching as shown in Figure 2.2. As noticed in the I-V curve, set and reset of the device is happening irrespective of the polarity of forcing node. A device in an HRS state can be switched to LRS state by a threshold voltage (V_{TH}) and the current is limited by compliance current (CC) to avoid hard break down in the switching layer of the device. Resetting back to ON-state happens at a same polarity below its V_{TH}. A much higher current can be observed in retting state of the device. Application of CC is not needed in retting of the device. Therefore, both the transition of setting and resetting are possible on both sides of the polarity.

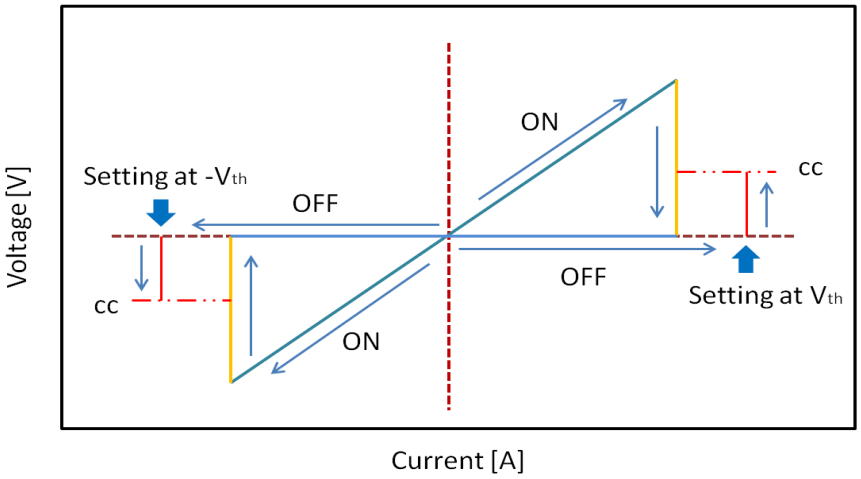

Figure 2.2 Amplitude dependent unipolar resistive switching.

2.1.2.2 Bipolar Memristors

The behavior of the device in which setting and retting of the device appeared at different sides of the polarity is termed as bipolar resistive switching. In this type of resistive switching, ON-state of the device occurs at some V_{TH} and OFF-state of the device occurs at some specific V_{TH} on the opposite side of the voltage polarity as shown in Figure 2.3. Bipolar resistive switching is also called polarity dependent resistive switching. Current observes in bipolar resistive is much lower as compared to that of unipolar resistive switching.

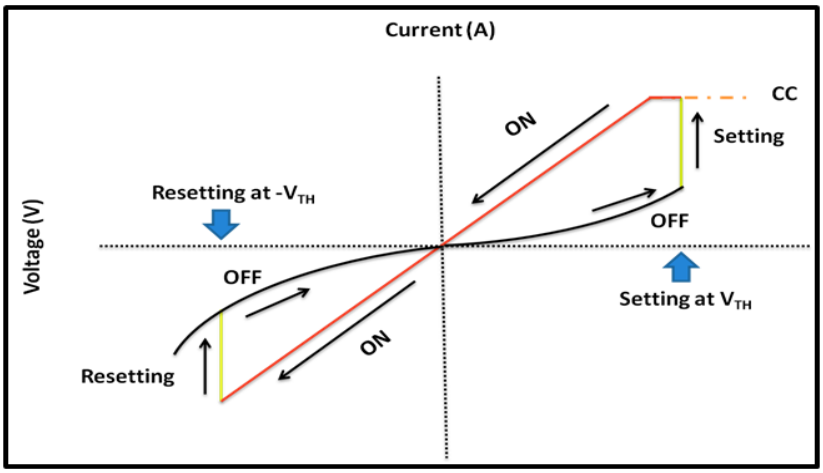

Figure 2.3 Polarity dependent bipolar resistive switching

2.1.3 Memristors Mechanisms

Several studies have been conducted for memristive mechanisms involved in metal oxides and polymers based sandwiched structures (Waser and Aono 2007, Sawa 2008, Akinaga and Shima 2010, Lee and Chen 2012, Cho et al. 2011, and Ling et al. 2008). Broadly, the purposed mechanisms are categories into two classes: the bulk effect and the interface effect.

2.1.3.1 Bulk Effect

The memristive effect that is caused by formation and rupturing of the conductive filaments due to joule heating in the sandwiched material between the two electrodes is termed as bulk effect or thermal effect. Bulk effect is observed common in unipolar resistive switching devices. Forming voltage is usually needed in these types of resistive switching. The filaments are formed by the voltage induced partial dielectric breakdown. These filaments may be composed of electrode material transported into the sandwiched layer, local degradation of the organic film or decomposed insulator material such as sub-oxides. During the resetting state of the device, the filaments are undergone into the rupturing phase hence the device change its LRS into HRS.

2.1.3.2 Interface Effect

Interface effect is common in bipolar devices. Different models are involved to explain the interface effect in bipolar resistive switching devices. Some common models are explained with the charge injection and trapping of charges in the traps in the insulator/oxide switching material. Traps play important rule when the interface between metallic/conducting electrode and insulator/oxide is schottky. When external potential is provided then the injected charges are trapped in the interface

between conducting electrode and insulator. When sufficient number of charges are gathered in the trap site eventually the scenario overcomes the barrier between metal-insulator interface and large current starts to flow through the interface. Contrary when the biasing is reversed then again the schottky barrier establishes and changes the device state to its original HRS.

2.1.3.3 Redox Process Induced Cation Migration

This model is based on the redox reaction of the metallic electrode. When one of the electrodes is chemically reactive while the other conducting electrode is inert then cations migrate in the ionic conductor. Chemically reactive electrode (Ag or Cu etc) undergoes oxidation reaction when force with some potential. The drift of cations (such as Ag^+ or Cu^+ etc) in the ion-conducting layer and their discharge at the counter electrode form a highly conductive path results in setting the device into the ON state. When the polarity is reversed, the conductive path undergoes into the electrochemical dissolution and resetting the device into the OFF state.

2.1.3.4 Redox Process induced Anion Migration

Anion migration model is based on the chemical redox reaction of insulator/oxide. This is the mechanism in which resistive switching takes place by the migration of anion/oxygen ion towards anode or better described by the migration of oxygen vacancies towards cathode. This model is also termed as oxygen vacancy migration resistive switching model. The migration of anion (oxygen ion) or oxygen vacancy leads to the change in stoichiometry and a valance change of the cation sub lattice. Eventually the state of the device changes to the LRS by the change in the electronic conductivity of the oxide/insulator.

2.1.3.5 Formation and Disruption of Metal Oxide

In some of the reports, the resistive switching effect was attributed to the formation and disruption of the metal oxide between the metallic electrode and oxide interface. When a potential is applied to the device, metal oxide formed due to the electrochemical reaction between the electrode material and sandwiched layer.

2.2 ZrO2: PVP Nano-composite based Memristor

For the first time, theoretical concept of fourth missing component of electronic circuits named as memristor was invented by Lean Chua in 1971 [1] Later on in 2008, HP group realized it physically using TiO2 material [2]. Memristors can sustain its high or low resistance state even after disconnecting the external power supply [3]. Due to this nonvolatile behavior and simple structure, memristor is considered as a proficient candidate to replace the main building block of electronic circuits named as transistor. Memristors have the wide range of applications and can be used in logic gates [4], Neuromorphic [5], and frequency selective circuits [6]. In expect of device stability, active layer material between two metal electrodes is very decisive for resistive memory devices. For this purpose, many researchers are working on different kind of materials for resistive memory devices like oxides [7], organic [8, 9], inorganic [10], nano-composite [11] and heterojunction [12]. Among these, the memory devices based on organic-inorganic nano-composite have great advantages due to hybrid properties, longer life time, high conductivity, and thermal stability [13]. Inorganic materials are widely used in realization of memory devices [14] but use of inorganic materials for memory devices have certain disadvantages as compare to organic material, as inorganic material requires high temperature processing for sintering [15]. On the other hand, the organic materials are flexible

due to long chain structure, longer life time in term of device stability, easy solution processing, and device fabrication at low temperature [16]. The properties of inorganic materials can be enchased by making organic-inorganic nano-composite materials [17]. Organic-inorganic nano-composite has a wide range of applications, due to its tunable optical, hybrid, electronic, and magnetic properties for electronic devices [18-20]. Hence, researchers are more focusing to fabricate resistive memory devices with nano-composite materials of organic-inorganic materials, which have properties of both organic and inorganic materials [21]. Addition of organic materials reduces the curing temperature and also no need for the high sintering temperature as we can fabricate the uniform film with composite materials.

In our work, we propose a resistive switching device with organic-inorganic nano-composite of Poly (4-vinylphenol) (PVP) and zirconium oxide (ZrO_2). Uniform film fabrication and the ease of processing is the key aspect of the proposed memory device using ZrO_2: PVP nano-composite with simple spin coating technology. The ZrO_2 is a metal oxide and exhibits bipolar resistive switching [22-23] and PVP has been selected to form nano-composite with ZrO_2 for many reasons: PVP is an organic polymer with insulator properties which helps in the fabrication of uniform film due to its long chain structure which also makes it highly transparent and flexible in nature. It is reported in different electronic devices [24-25]. The stability of memory device is an important feature, and we mixed ZrO_2: PVP in different blending ratios 1:0, 1:0.25, 1:0.5, and 1:1 to study the effect of adding PVP on the switching properties of ZrO_2. The PVP restricts the agglomeration of ZrO_2 in the solution that results in a uniform deposition of thin film using spin coater. The resistive switching mechanism of ZrO_2: PVP is explained with the help of controlled space charge limited current (SCLC) model. The higher resistance state (HRS) and

lower resistance state (LRS) are recorded as following 11.438 kΩ and 263.25 Ω, respectively. The surface morphology of memory device is analyzed by Jeol JSM-7600F FE-SEM, and a chemical Investigation of active layer is performed with Lab Ram HORIBA spectrometer, elemental composition can be confirmed by using energy dispersive X-ray spectroscopy (EDS) and electrical characterization is performed with KEYSIGHT B2902A source measuring unit. In the paper, the material and fabrication process is given in section 2, device characterization is given in section 3, result and discussion is given in section 4, and conclusion is given in section 5.

2.2.1 Material and Fabrication

Fig. 1 shows the layer by layer layout schematic of resistive memory device, which consists of Ag as top electrode and ZrO_2: PVP as an active layer, and ITO as a bottom electrode. For the fabrication of memory device, we required following materials Zirconium oxide (ZrO_2) nano-particles 5% dispersion in water (H_2O), Poly (4-vinylphenol) (PVP) average Mw ~25,000, Poly(acrylic acid) partial sodium salt solution average Mw~5,000, Ag ink with 50% dispersion in tripropylene glycol mono methyl ether (TGME), Dimethylformamide (DMF), and Indium tin oxide (ITO) coated PET with surface resistivity of 60 Ω/sq were purchased from sigma Aldrich, South Korea. The conductive Ag epoxy CW2400 purchased from circuitsworks to fabricate top electrodes. The ZrO_2 nano-particles ink with 5% dispersion of in H_2O is mixed with DMF in 1:1. The 0.1% PAA was used as dispersant. The ZrO_2 ink was probe sonicated for 10 min with frequency of 19.8 kHz, which was magnetic stirred for 8 hrs at rate of 1200 rpm at 60 ^oC. Then it was bath sonicated for 30 min. It results in the formation of white dispersion of ZrO_2 nano-particles and it was filtered by using 2 μm filter paper. Then, we prepared another solution which contain 10 ml

of DMF and 0.1 g of PVP, it was placed on magnetic stirring for 2 h at the rate of 1500 rpm, bath sonicated for 30 min, probe sonicated for 10 min and centrifugation for 2 min at 3000 rpm. We performed experiments with different blending ratio of ZrO_2 and PVP, we got best result with the blending ratio of 1: 0.5 by using spin coating technique.

The fabrication process of proposed memory devise is shown in Fig. 2.4. Prior to the fabrication process, ITO coated PET was cleaned with acetone and de-ionized water and placed in UV treatment box for 10 min. The fabrication process consists of following steps; (i) fabrication of active layer and (ii) fabrication of top electrode. In first step, using ZrO_2: PVP nano-composite, an active layer is fabricated through spin coating technique on ITO coated PET substrate at 2500 rpm for 35 sec and cured at 120 ^oC for 2 h. In the second step, 100 µm thickness Ag as top electrodes are patterned by using Ag epoxy and cured at 60 ^oC for 60 min.

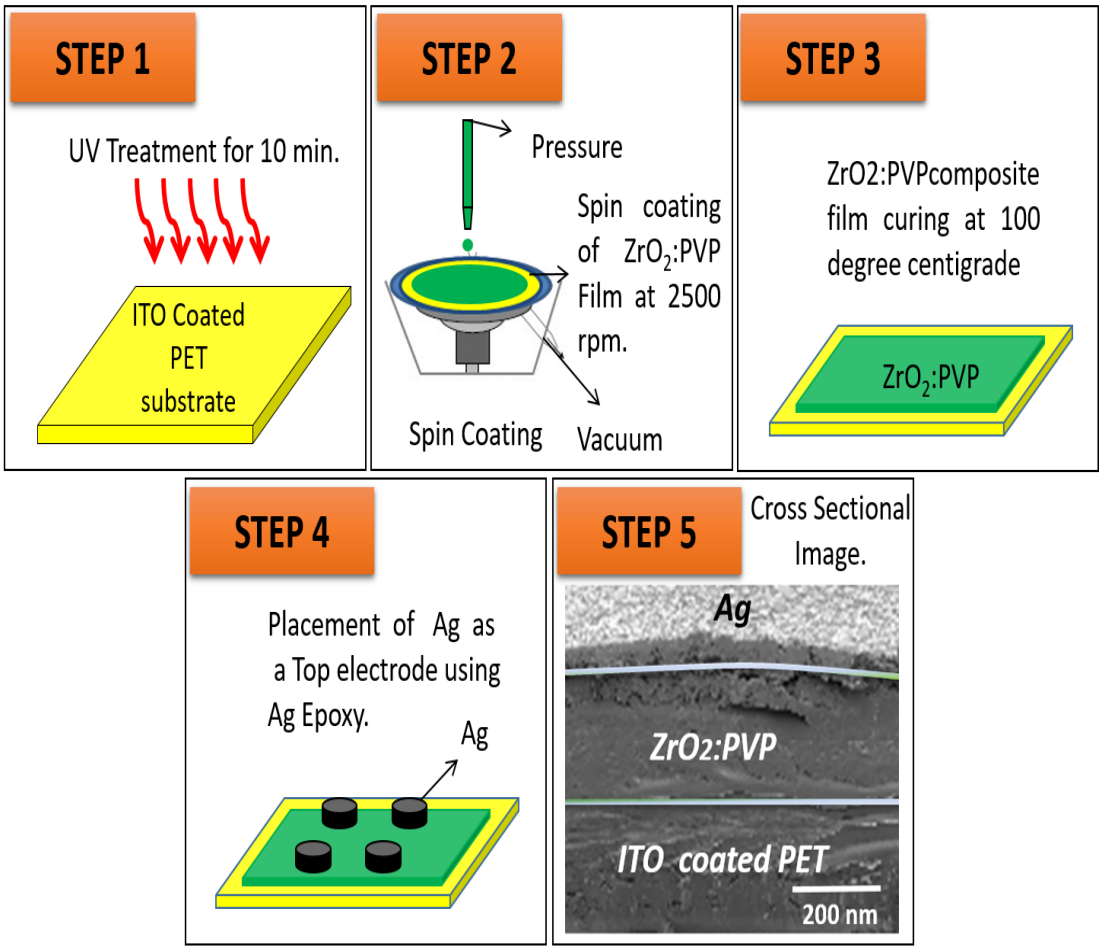

Figure 2.4 a) Fabrication process of memory device and the Cross sectional image of ITO/ZrO2: PVP/Ag resistive memory device with 200 nm magnification.

2.2.2 Characterization

The surface morphology of active layer and top electrode were analyzed by scanning electron microscope (SEM) Jeol JSM-7600F, structural and chemical investigation of PVP, ZrO_2, and ZrO_2: PVP nano-composite films were tested by Raman spectroscopy

(Lab Ram HORIBA spectrometer), elemental determination was analyzed on an energy dispersive X-ray (EDS) spectrometer attached to the FESEM. The samples were coated by platinum (Pt) sputter coater and I-V characteristics of device were also recorded with KEYSIGHT B2902A precision source/measure unit.

Fig. 2.4 shows the cross sectional image of the fabricated device with thickness of 200 nm. It ensures that the active layer is properly fabricated through a spin coater.

The SEM image of Ag, ZrO2, PVP and ZrO_2: PVP nano-composite are shown in Figs. 2.5 a, 2.5c, 2.5e and 2.6a, respectively, which indicate that all layers are uniformly fabricated with a spin coater. The elemental compositions of the Ag and ZrO_2: PVP nano-composite were obtained using energy dispersive X-ray spectroscopy (EDS) analysis during SEM as depicted in Figs. 2.5 b and 2.6b. EDS spot profile of the silver shows the sharp peak of Ag as shown in Fig. 2.5a. Fig. 2.6b show the EDS spot profile for the ZrO_2: PVP nano-composite, which clearly show peaks of Zr, O, and C, where the C peak is from PVP, while Zr and O peaks are from ZrO_2. Raman spectroscopy was carried out to confirm structural and chemical investigation of PVP and ZrO_2 as shown in Figs. 2.5d and 2.5f. The deposited PVP film through a spin coater has two characteristics as broader peaks around 500 cm^{-1} and 800 cm^{-1} as Raman spectrum shown in Fig. 2.5d, while there indicate few medium and narrow peaks at different Raman shifts [26]. In Fig. 2.5f, ZrO_2 exhibits characteristic a narrow peak at 150 cm^{-1}, broader peak at 265 cm^{-1}, medium and weak peaks at 315 cm^{-1}, 460 cm^{-1}, and 650 cm^{-1} [27, 28].

Fig. 2.6c shows the EDS mapping of ZrO_2: PVP nano-composite, which illustrate the element composition of Zr, O, and C. The C peak is from PVP, while Zr and O peaks are from ZrO_2. The content of zirconium with their corresponding amount of oxygen and carbon are 42.99 wt%, 34.06 wt%, and 22.94 wt% as shown in Fig. 3b, which indicate proper incorporation of PVP into ZrO_2 in Figs. 2.6d, 2.6e, and 2.6f.

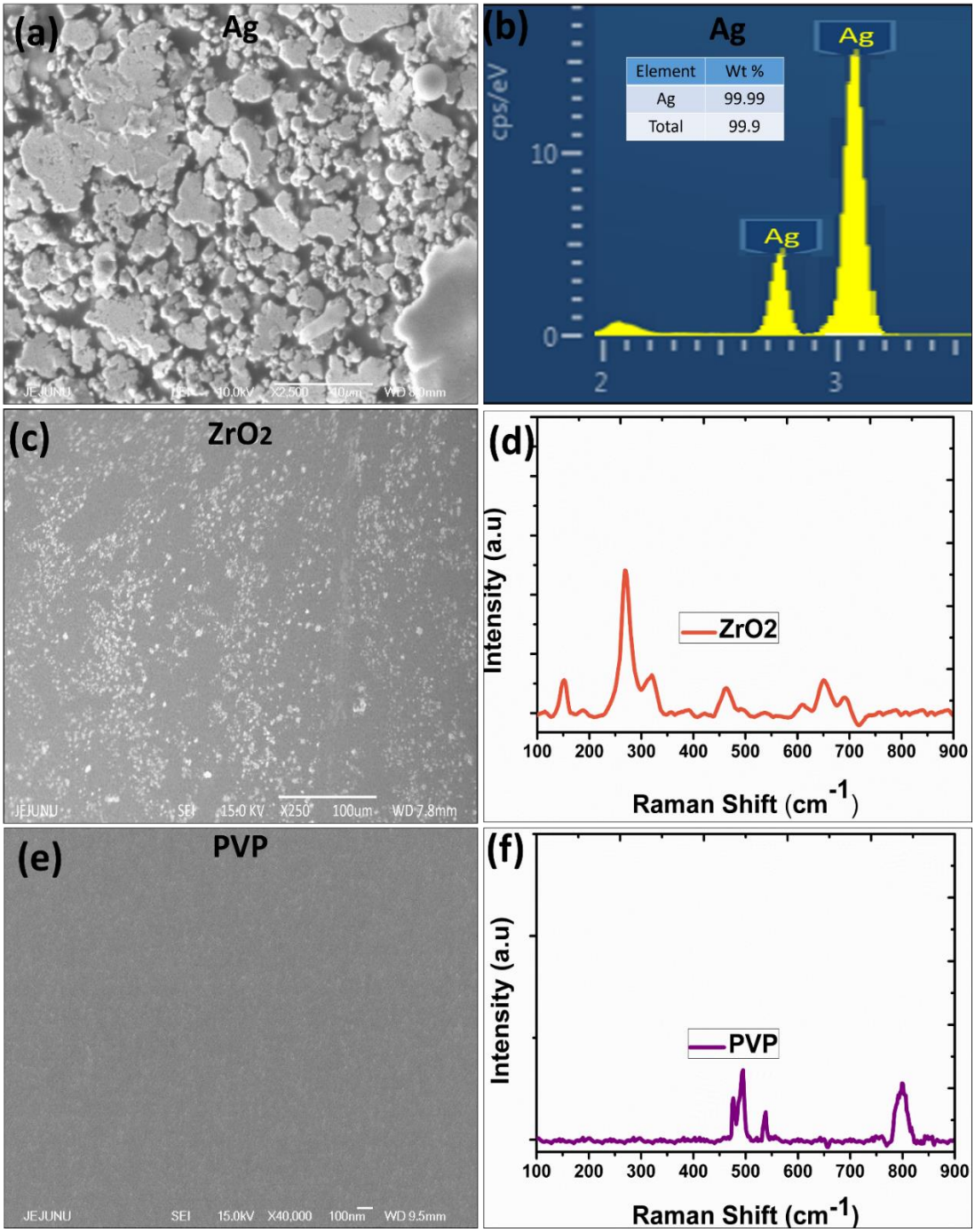

Figure 2.5 Surface morphology of (a) Ag, (c) ZrO2, and (e) PVP film are uniformly deposited through a spin coater. EDS spectra of (b) Ag and Structural characterizations of (d) ZrO2 and (f) PVP.

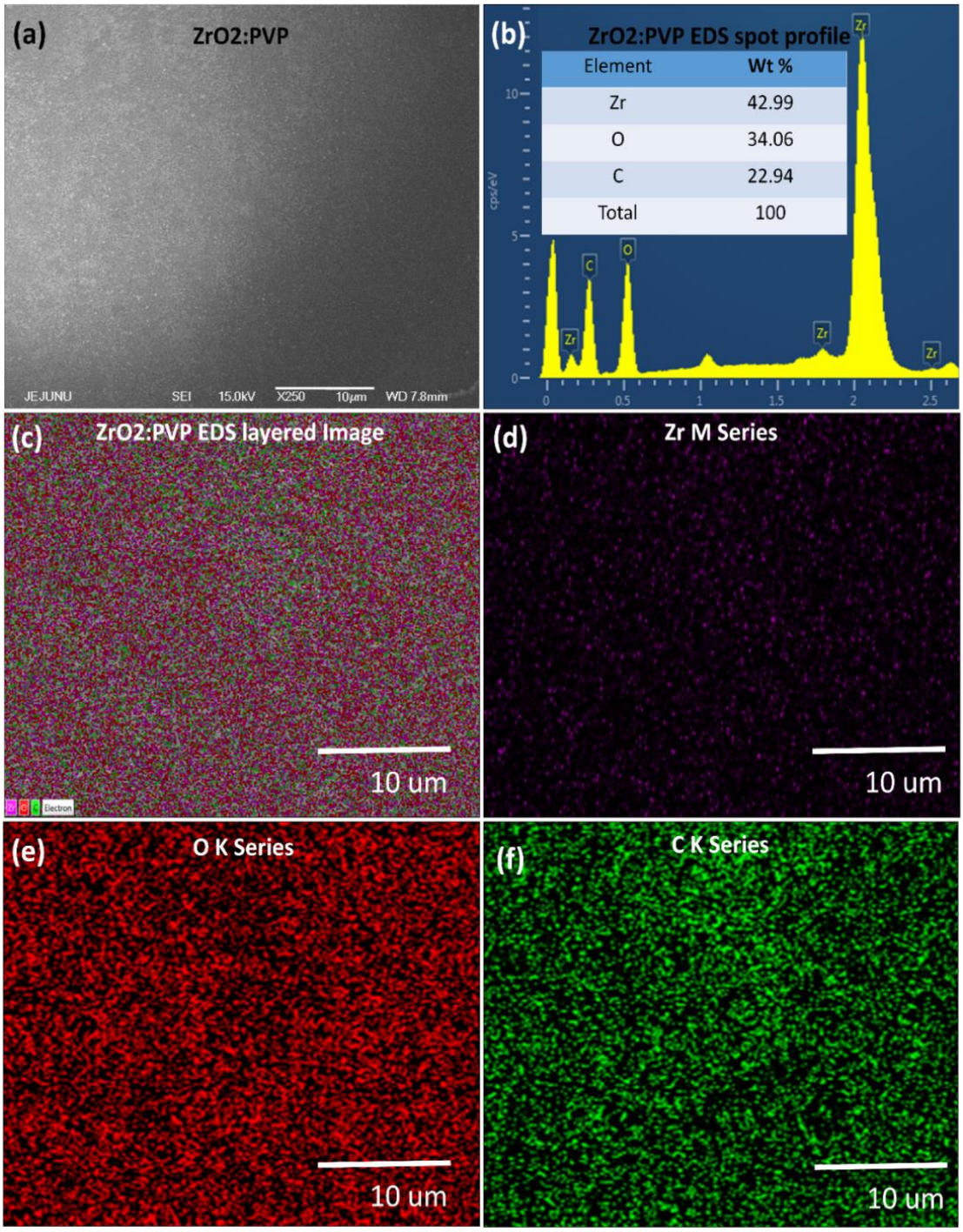

Figure 2.6 (a) SEM of ZrO2:PVP Nano-composite. (b) EDS spot profile of ZrO2: PVP Nano-composite, EDS layered image of ZrO2: PVP Nano-composite showing (d) zirconium, (e) oxygen and (f) carbon.

For electrical characterization, we placed the fabricated device ITO/ZrO_2/Ag in a Probe station for current and voltage (I-V) characterization by using software controlled KEYSIGHT B2902A source measuring unit. The samples were biased with voltage sweep of ±1.5 V as shown in Fig. 2.7a.

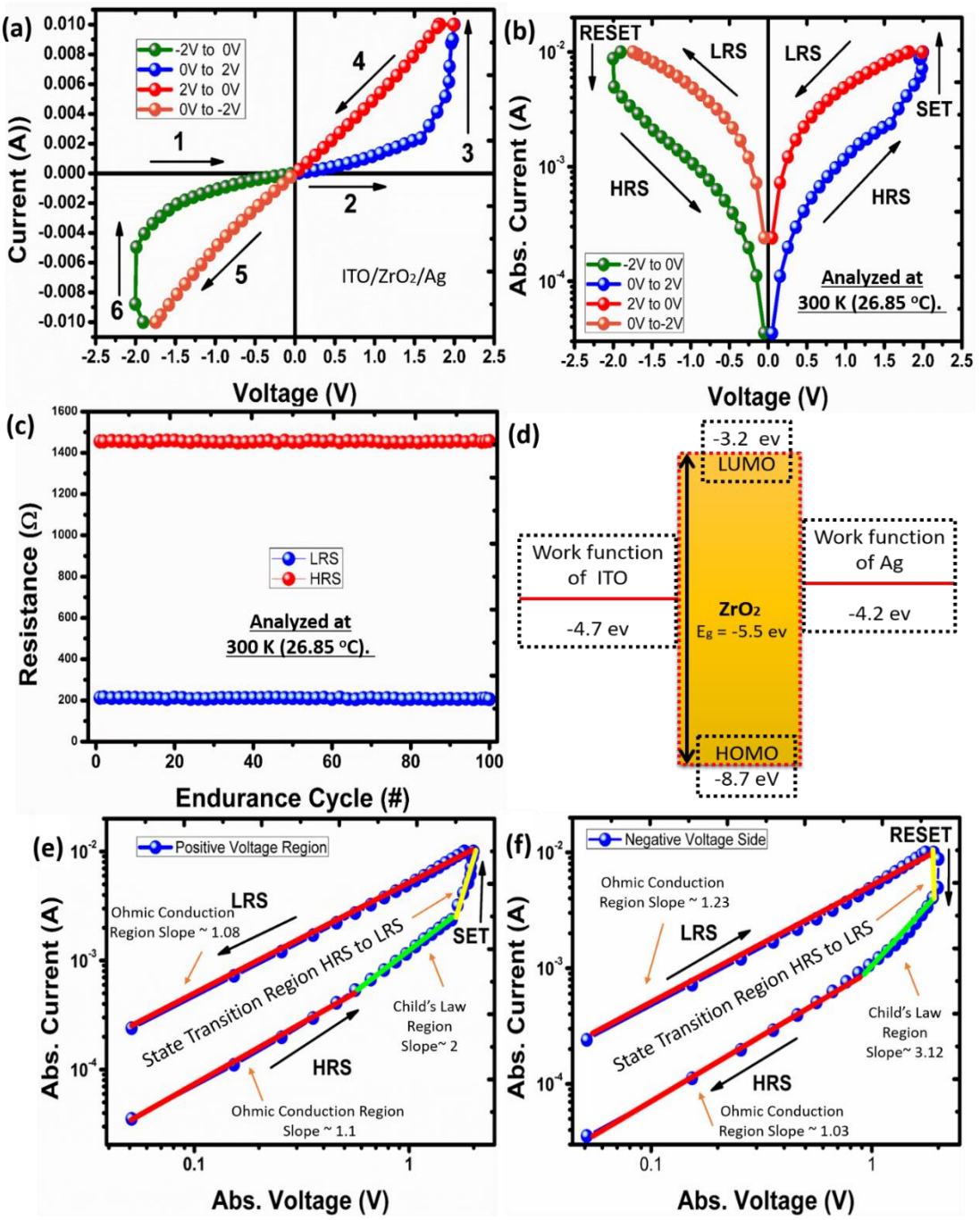

Figure 2.7 (a) Electrical characterization of the proposed resistive memory device ITO/ZrO2/Ag, (b) semi log image. TCSCLC mechanism, of (c) positive voltage side, (d) negative voltage side, (e) Energy band diagram of ITO/ZrO2/Ag.

The ITO/ZrO2/Ag memory device exhibits stable resistive switching and Fig. 2.7b shows the bipolar resistive switching behavior and device endurance shown in Fig. 2.7c. The energy band diagram mechanism based on HOMO and LUMO of ZrO_2 is explained in Fig. 2.7d, where HOMO and LUMO are -3.2 eV and 8.7 eV, respectively. The charge trap controlled space charge limited current (TCSCLC)

mechanism of ITO/ZrO2/Ag is explained in Fig. 2.7e and 2.7f with double log current and voltage graph. The high resistance state (HRS) 1446.12Ω and low resistance state (LRS) 212.76 Ω with the R_{off}/R_{on} ratio of the memory device ~ 6.79 at voltage read of 0.05 V and the detection margin between HRS and LRS is very low. In order to improve the R_{off}/R_{on} ratio of memory device we prepare nano-composite of ZrO_2 with PVP with different blending ratios like 1:0, 1:0.25, 1:0.5, and 1:1 as shown in Fig. 2.8a and 2.8b. We optimized the blending ratio of ZrO_2:PVP by using 1:0.5 and we fabricated the resistive memory device ITO/ZrO2:PVP/Ag and it was biased with ±1.5V.

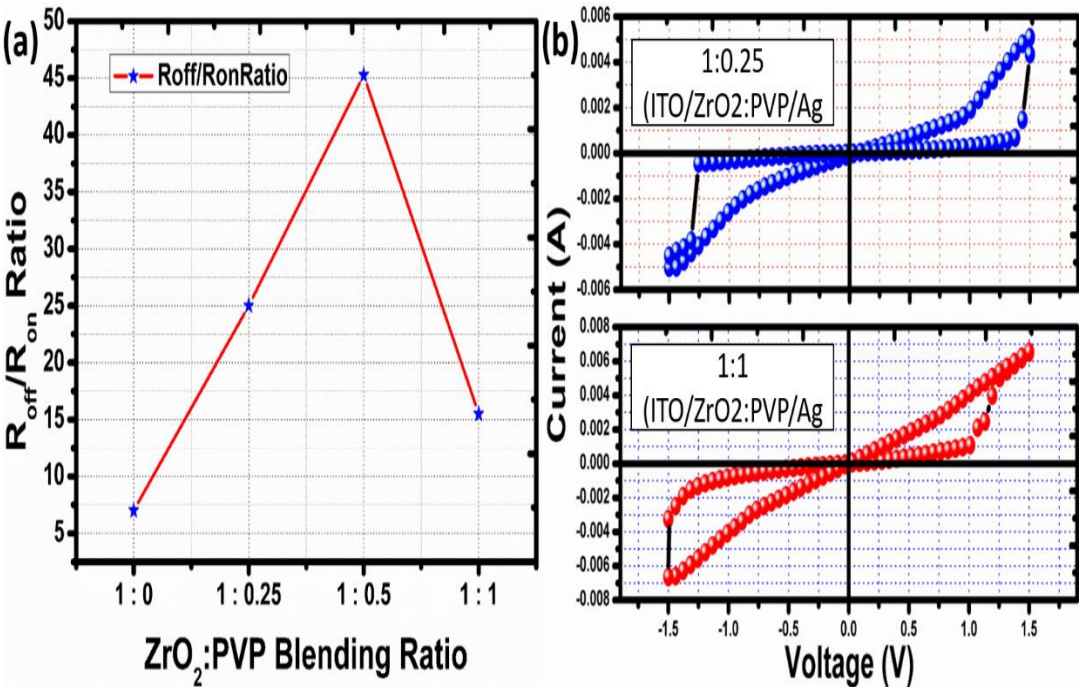

Figure 2.8 (a) Roff/Ron ratio analysis of ZrO2:PVP (b) I-V curve of blending ratio 1:0.25 and 1:1.

During dual voltage sweep from -1.5 to 1.5 V as shown in Fig. 2.9a, the proposed memory device remains in HRS under 1.4 V, but after threshold voltage current is abruptly increased and the state is shifted from HRS to LRS (SET). Similarly, under reverse voltage sweep of 1.5 to -1.5 V, the resistive memory device remains in LRS, and memory device shift from LRS to HRS (reset) at -1.4 V, and decrease in current

is observed and memory device comes back to HRS and It is maintained until reverse voltage sweep is not applied. The proposed memory device repeats the same process in each cycle. Fig. 2.9b shows the semi-log scale I-V curve of ITO/ZrO_2: PVP/Ag memory device and it insures that memory device is passing through zero volts and exhibits the bipolar resistive switching behavior at dual bias voltage ±1.5 V. As shown in Fig. 2.9b, during voltage sweep of -1.5 to 1.5 V, the memory device has HRS and very less amount of current passes in HRS. Over the threshold voltage device, it goes in set process from HRS to LRS and current is abruptly increases. During reverse voltage sweep of 1.5 to -1.5 V, device under goes in LRS. The current is abruptly decreased at negative threshold voltage and the memory device is shifted from LRS to HRS (RESET). The HRS and LRS are recorded as following 11.438 kΩ and 263.25 Ω, respectively and the R_{off}/R_{on} ~ 44.

The mechanism of the proposed device can be explained with the help of log-log I-V graph as shown in Figs. 2.9c and 2.9d. These results are comparable with other reported resistive switching mechanism in inorganic [29], organic [30], and nano-composites [31]. LRS shows the ohmic behavior with a slope value of ~ 1. However, HRS as off state shows the two different values of slopes (i) green marked region and (ii) red marked region as shown in Figs. 2.9c and 2.9d. To describe the current in HRS state, we need TCSCLC mechanism. The TCSCLC is divided into two regions as following; (i) due to thermionic emission, small electric field is created in linear ohmic conduction region ($I \propto V$) (green marked region) and (ii) the electrons present in electrode get enough energy and these charges start entering toward active layer of ZrO_2: PVP nano-composite in child's law region (red marked region). After that resistive memory device switches from HRS to LRS in orange marked region represents the state transition region, it follows by the relation of current and applied

voltage ($I \propto V^n$) as shown in Figs. 2.9c and 2.9d. The conduction filaments are formed in ZrO_2: PVP nano-composite due to the migration of the induced charge carriers from Ag electrode and ZrO_2 nano-particles act as a charge trapper and PVP act as a charge blocking material as shown in Fig. 6c. This process can be explained using the energy band diagram based on the highest occupied molecular orbit (HOMO) and lowest unoccupied molecular orbit (LUMO) based on ZrO_2 and PVP as shown in Fig. 2.9e. The HOMO and LUMO values of PVP (-06.4 eV and -2.4 eV) [32] and ZrO_2 (-8.7 eV and -3.2 eV) [33], respectively. The work function of ITO and Ag are -4.7 eV and -4.2 eV, respectively. For the applied voltage less than the threshold voltage, low current passes through the active layer due to an insulator property of PVP with energy band gap (E_g) of ~4.0 eV, which corresponds to the HRS state of memory device. The induced charge carriers from the Ag electrode are trapped inside the ZrO_2 nano-particles. Due to the high band gap of ZrO_2 E_g is ~ -5.5 eV, and reduces the available traps, due to the high band gap difference of HOMO to HOMO of ~2 eV between ZrO_2 and PVP as compare to LUMO to LUMO difference ~1 eV. Depending on the polarity of the applied voltage, the density of free electrons increases due to trapping of charge carries. Hence a conduction channel will form and electrons will move from HOMO of PVP to HOMO of ZrO_2 or HOMO of ZrO_2 to HOMO PVP.

Fig. 2.9f shows the temperature dependency of memory device from 300 K to 350 K, which can be clearly seen that with increase in temperature LRS of memory device increases due to filament formation and positive temperature coefficient of metals. The HRS of resistive memory device decreases with increase in temperature due to negative temperature coefficient of semiconductor nature of material in an active layer [34-35]. When the power source is turned off, the high dielectric and insulator

property of PVP enhances the capping effect on ZrO_2, which does not allow the charge carrier to move back to their normal energy state with low conductivity by restricting them in trapped state.

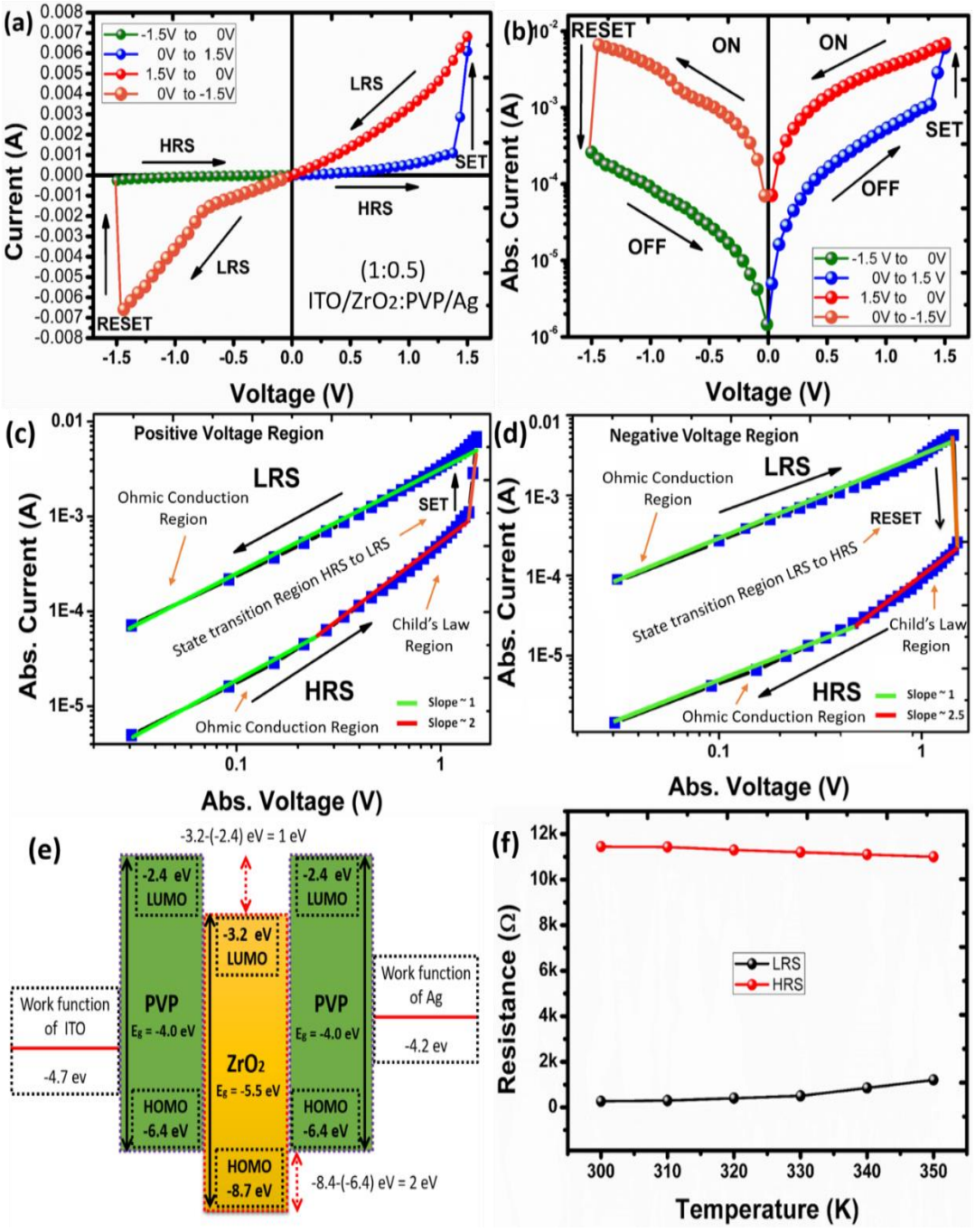

Figure 2.9 (a) I-V curve of ITO/ZrO2: PVP/Ag Nano-composite, (b) Semi-logarithmic I-V curve, which illustrates a stable bipolar resistive switching of memory device. The charge trapping mechanism is explained using double log I-V curve of (c) positive voltage side

The memory device is continuously tested for more than 200 endurance cycles, and it shows a stable memristor function with any invariable changes in resistance state (HRS and LRS) at room temperature 300 K (26.85 ^{o}C). As the semi-log graph of I-V shown in Fig. 2.10a, it shows the continuity of memristor for 1st, 100th, and 200th cycle. The HRS and LRS are tested for more than 200 voltage sweep as shown in Fig. 2.10b, which show stable memory functions. The time duration for which device can hold its data without any power is called retention time. To evaluate the retention time, the fabricated device was set under observation over 30 days, and its retention time were tested as shown in Fig. 2.10c, which show a stable bipolar resistive switching behavior. The stability of the proposed memory device without any significant changes in HRS and LRS was observed for more than 30 days as shown in fig 2.10d.

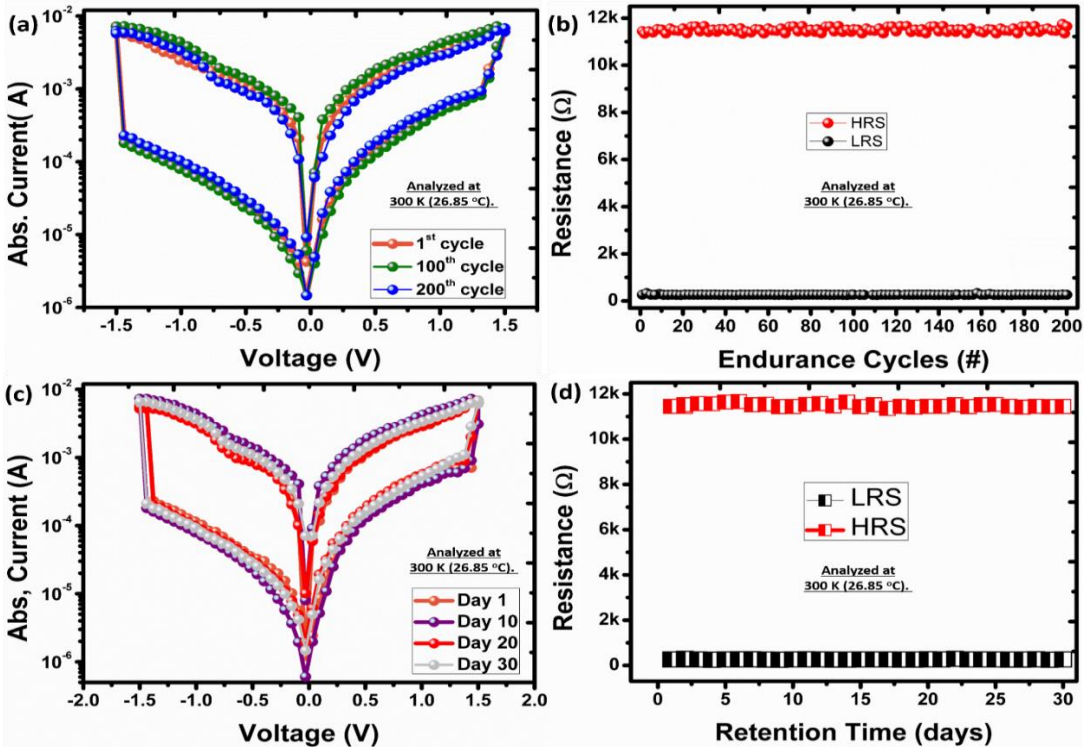

Figure 2.10 (a) Semi-logarithmic I-V curve showing the stability of the proposed memory device for 1st, 100th, and 200th switching cycles. (b) The memory device switching between HRS and LRS during dual biased voltage of ±1.5 V, and it shows a stable switching beha

The mechanical properties were analyzed by bending it on flat surface (see Fig. 2.11a), and diameters of 30 mm (see Fig. 2.11b) and 10 mm (see Fig. 2.11c) with indigenously made bending setup as shown in Fig. 2.11. Here, the minimum bending diameter is 10 mm as shown in Fig. 2.11d and it is open circuited beyond 10mm, due to micro carks appear on the top of the active layer.

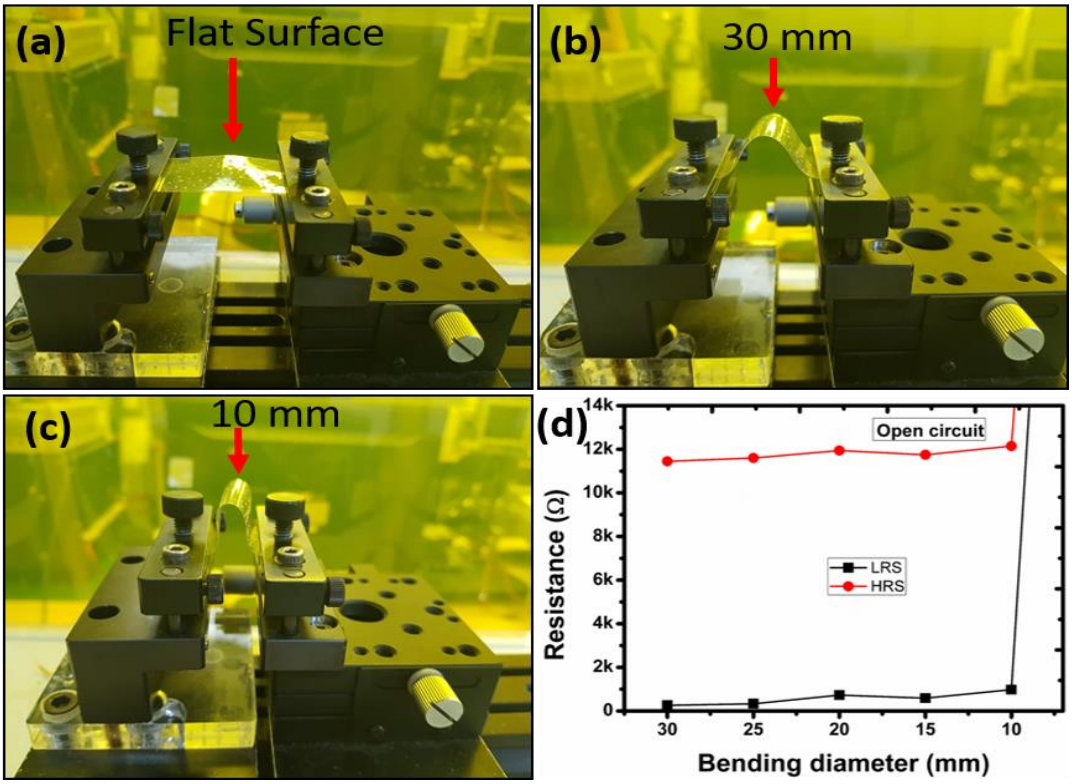

Figure 2.11 The Mechanical robustness of memory device is tested by using bending machine on (a) flat surface, (b) bending diameter of 30 mm and (c) bending diameter of 10 mm. (d) Beyond 10 mm, it become an open circuit

2.2.3 Summary

We have fabricated the non-volatile resistive switching memory device based on ZrO_2:PVP organic-inorganic nano-composite on ITO coated PET substrate and Ag epoxy was used as top electrode. Active layer was fabricated through Spin coater. The proposed memory device operates at voltage sweep of voltage ±1.5 V. The SEM image indicated that active layer of ZrO_2:PVP nano-composite was uniformly fabricated through spin coating technology. The EDS spot profile and mapping of nano-composite have confirmed the presence of ZrO_2 and PVP in organic-inorganic

nano-composite. The mechanism of the fabricated device was explained by space charge limited current and energy band diagram mechanism based on HOMO and LUMO. We have achieved R_{on}/R_{off} ratio ~44.

2.3 Bilayer resistive switching device based on N, N′-Bis (3-methylphenyl)-N, N′-diphenylbenzidine (TPD) and Poly (3,4-ethylenedioxythiophene) poly (styrenesulfonate) / Poly (vinyl alcohol) (PEDOT:PSS/PVOH) composite.

In 1971, Leon Chua for the first time presented the mathematical model of memristor [36] and later it was physically realized by HP group in 2008 [37], which is also called resistive switching device. After that, the memristor is considered as a fourth component of electronic circuits that directly relates the relationship of charge and flux [38]. It exhibits the non-volatile resistive memory behavior, due to the movement of the charge carrier in an active layer [39]. Nowadays, the resistive switching device has got tremendous attention due to its wide range of applications such as non-volatile resistive memory [40, 41], computing [42], data logic [43], frequency selective circuits [44, 45], and synapses [46,47]. In this expectation, it is a competent candidate to replace the main building block of the electronic circuits named as transistor [48].

There are many challenges to fabricate resistive memory devices like switching speed, R_{off}/R_{on} resistance ratio, current density, stability, and retention time. To overcome these challenges, many researchers are utilizing single material like metal oxides [49-52], bio materials [53, 54], composite materials [55, 56], organic materials [57, 58] based on electroforming [59], filament formation [60], and ion migration [61]. To design an active layer, organic materials are more preferred due to

device stability, long chain structure, easy material processing, low cost, longer life time, and low temperature processing [62-64]. Many researchers are exploring new materials for non-volatile resistive memory with a bilayer structure of two different materials based on ion migration and defects [65-68]. Based on different type of materials, the bilayer structures are proposed for the fabrication of the various memory devices like Ag/PMMA/MEH:PPV/Ag, Pt/BiFeO3/Nb-doped SrTiO3 heterostructure and Ag/PEDOT:PSS-PVP/Methyl red/Ag bilayer structure [69-71]. To improve the current density and R_{off}/R_{on} ratio of a bilayer resistive memory device [72], new materials are required to be explored.

To explore a new bilayer non-volatile resistive switching device, this paper proposes the resistive switching device with a bilayer stacked structure based on N,N′-Bis(3-methylphenyl)-N,N′-diphenylbenzidine (TPD) and Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate)/ Poly(vinyl alcohol) (PEDOT:PSS/PVOH). Here, the TPD is an organic photo conductor polymer having the semiconductor property with a high hole mobility of 1×10^{-4} cm^2/Vs, and it is widely used in solar cells as photoconduction and laser devices [73]. TPD is applied for first time for the resistive switching device in this paper. The PEDOT: PSS is a conducting polymer with conductivity >200 S/cm [74] with positive charge Poly (3,4-ethylenedioxythiophene) (PEDOT), which is cationic polythiophene derivative and negative charge poly (styrenesulfonate) (PSS). It is well known as polyanion and it is widely used in OLED [75] and transparent electrode [76] due to charge transport property [77]. Due to a high band gap of PVOH, it offers a high dielectric and insulator property [78]. The R_{off}/R_{on} ratio of the proposed device can be improved by using PVOH and PEDOT:PSS composite. Utilizing the composite, the high resistance state (HRS) value can be increased; hence we can design the

difference between HRS and low resistance state (LRS) to increase the R_{off}/R_{on} ratio. The proposed bilayer resistive switching memory device based on the TPD and the (PEDOT:PSS/PVOH) composite is fabricated with a spin coating technique on indium tin oxide (ITO) coated PET substrate, and top electrode are patterned by using silver (Ag) epoxy. The R_{off}/R_{on} ratio of the proposed memory device is ~28.7 at voltage read of 0.58 V with HRS (97.23 kΩ) and LRS (3.38 kΩ). It maintains stable resistive switching for more than 300 cycles and retention time of more than 10^4 sec. For the device characterizations, several techniques are utilized to investigate its surface morphology, chemical and electrical characterizations.

2.3.1 Materials and Fabrication

For the fabrication of the resistive memory device, the TPD with Mw ~516.67 and PEDOT:PSS with 3% solid content in water (H_2O), PVOH with Mw 9,000, Ethanol, Toluene, De-ionized water, ITO coated PET with surface resistivity of 60 Ω/sq were purchased from Sigma Aldrich, South Korea. The ink of the TPD is prepared as: the 10 wt% TPD was dissolved in toluene. The PEDOT: PSS with 3% solid content was mixed with 10 wt% in de-ionized water. Then, we prepared another solution using PVOH of 5 Wt% in de-ionized water. All prepared inks were placed on magnetic stirrer for 2 hr at 1000 rpm and bath sonication was run for 30 min. For a high R_{off}/R_{on} resistance ratio, a high resistive material is required, but the PEDOT:PSS is less resistive material in itself. For this reason, we added the PVOH material used as an insulator in nature, and the resistivity of the (PEDOT:PSS/PVOH) composite is increased. To get a best composite, we performed experiments with different blending ratios of PEDOT:PSS and PVOH, and its optimum blending ratio is 3:1. The proposed resistive switching memory device is fabricated by using spin coating technology as shown in Fig. 2.12. Before starting a fabrication process, an ITO

coated PET was cleaned with ethanol and washed with de-ionized water to remove the traces of ethanol and its substrate was placed in UV treatment equipment for 10 min to create surface roughness. The TPD film was fabricated through a spin coater at 1200 rpm for 30 sec and cured at 100 ^{o}C for 1 hr. Similarly, the (PEDOT:PSS/PVOH) layer was fabricated using the spin coater at 2000 rpm for 40 sec and cured at 100 ^{o}C for 2 hr. The top electrode was deposited on the active area of 100 µm by using Silver (Ag) conductive epoxy CW2400 purchased from circuits works. It was cured at 30 ^{o}C using heating furnace.

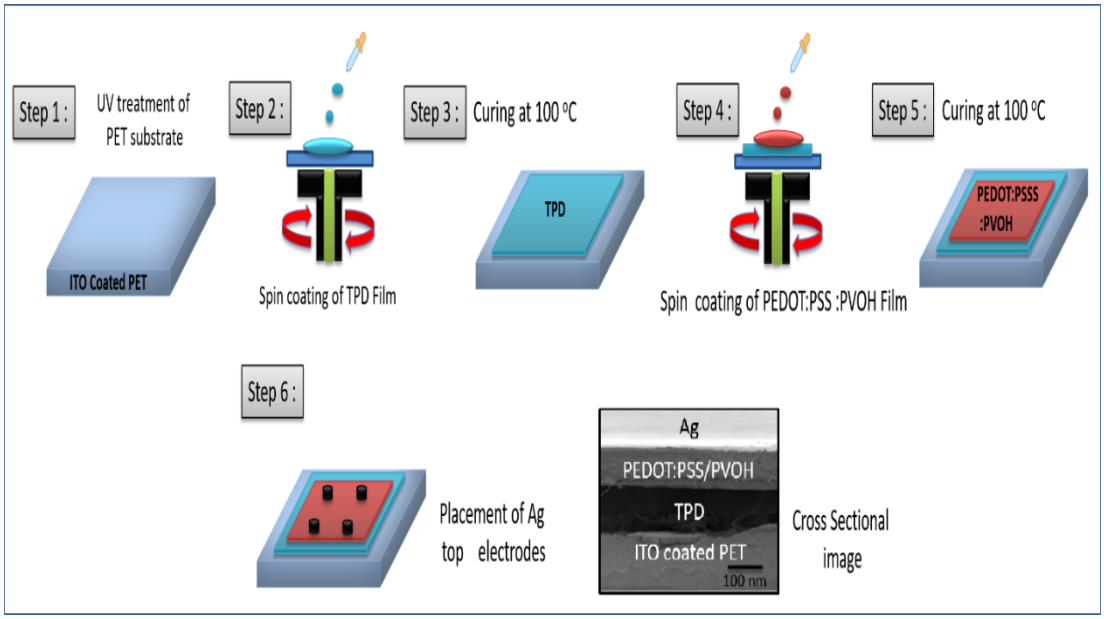

Figure 2.12 Fabrication process of the proposed memory device (ITO/TPD/(PEDOT:PSS/PVOH)/Ag) through the spin coater and the insert image shows the cross sectional image.

The surface morphology of the TPD and the PEDOT:PSS were analyzed by TESCAN MIRA 3 scanning transmission electron microscope (STEM) as shown in Figs. 2.12, 2.13(a), 2.13(b), and 2.13(c). The structural and chemical investigation of the TPDS and the PEDOT:PSS were tested with HORIBA spectrometer as shown in Figs. 2.13(d) and 2.13(e). Elemental composition of the (PEDOT:PSS/PVOH) can be confirmed by using energy dispersive X-ray spectroscopy (EDS) as shown in Fig.

2.13(f). The current and voltage (I-V) analysis of the proposed device was recorded by using KEYSIGH B2902A source measuring unit as shown in Fig. 2.14.

2.3.2 Characterizations

The surface morphology of TPD, PEDOT:PSS, and (PEDOT:PSS/PVOH) are uniformly fabricated with a spin coater as shown in Figs. 2.13(a), 2.13 (b), and 2.13 (c) with magnification level of 500 nm, respectively. Fig. 1 shows the cross sectional image, which ensures that the fabricated films are properly fabricated through a spin coater. Raman spectroscopy is a powerful tool to characterize thin films. The TPD and the PEDOT:PSS samples were characterized by using LabRam HR Evolution Raman spectrometer (Horiba Jobin-Yvon, France). This Raman spectroscopy was carried out to confirm chemical and structural investigation of the TPD and the PEDOT:PSS films, and both spectra were carried out between Raman shift ranges between 400 to 1800 cm^{-1} as shown in Figs. 2.13(d) and 2.13(e). As shown in Fig. 2.13(d), Raman spectrum of TPD film is dominated by several distinct peaks between 1000 and 1600 cm^{-1} due to plane elongation of phenyl rings, and few characteristics peaks are below 500 cm^{-1}. The bands at 1600 cm^{-1}, 1300 cm^{-1}, and 1200 cm^{-1} are attributed to carbon-carbon(C-C) intra-ring stretching, C-C inter-ring stretching, and carbon-hydrogen (C-H) bending mode [79, 80]. Whereas, the Raman spectrum of the PEDOT:PSS shown in Fig. 2.13(e) indicates most prominent peak between 1400 and 1500 cm^{-1}. The peaks at 1511cm^{-1} and 1568 cm^{-1} are characteristics of asymmetric Cα = Cβ stretching, while the peaks at 1444 cm^{-1} are symmetric Cα = Cβ stretching. The bands at 1258 cm^{-1} and 1373 cm^{-1} are attributed to Cα− Cα inter ring stretching and Cβ− Cβ stretching. Bands at 905 $cm^{-1}$and 582 cm^{-1} are attributed to oxy-ethylene ring deformation. The peaks at 1040 cm^{-1}, 708 cm^{-1}, and 446 cm^{-1} are characteristics of C-O-C deformation, C-S-C deformation, and

SO_2 bending, respectively [81]. The elemental composition of the (PEDOT:PSS/PVOH) composite was obtained using energy dispersive X-ray spectroscopy (EDS) analysis during SEM as depicted in Fig. 2.13(f). A spot-profile EDS of the (PEDOT:PSS/PVOH) composite clearly shows peaks of C, O, and S. The C and O peaks are from PEDOT:PSS and PVOH while S peaks are from the PEDOT:PSS.

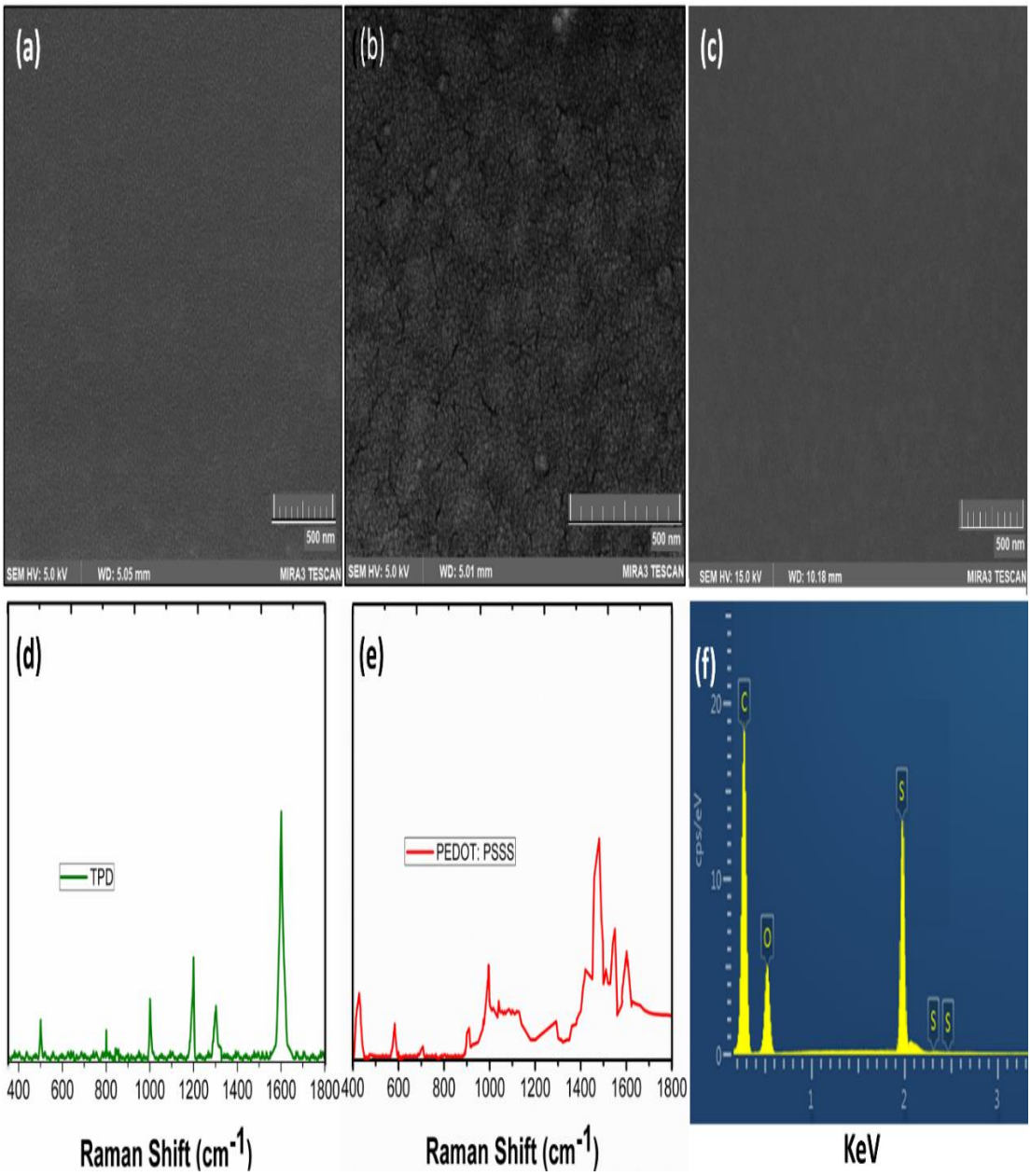

Figure 2.13 Surface morphology of polymeric materials are analyzed by scanning transmission electron microscope (STEM) TESCAN MIRA 3 with high magnification, (a) TPD, (b) PEDOT: PSS, (c) (PEDOT:PSS/PVOH) composite. The structural characterization of (d) TPD and (e)

To characterize TPD with KEYSIGHT B2902A source measuring unit, we applied voltage sweeping of ±2 V as shown in Fig. 2.14(a) with ITO coated PET as a bottom electrode and Ag as top electrode as the structure of ITO/TPD/Ag. However, it has not a resistive memory function. Similarly, we applied voltage sweeping of ±3 V for the structure, ITO/PEDOT:PSS/Ag as shown in Fig. 2.14(b), and it just shows an ohmic behavior.

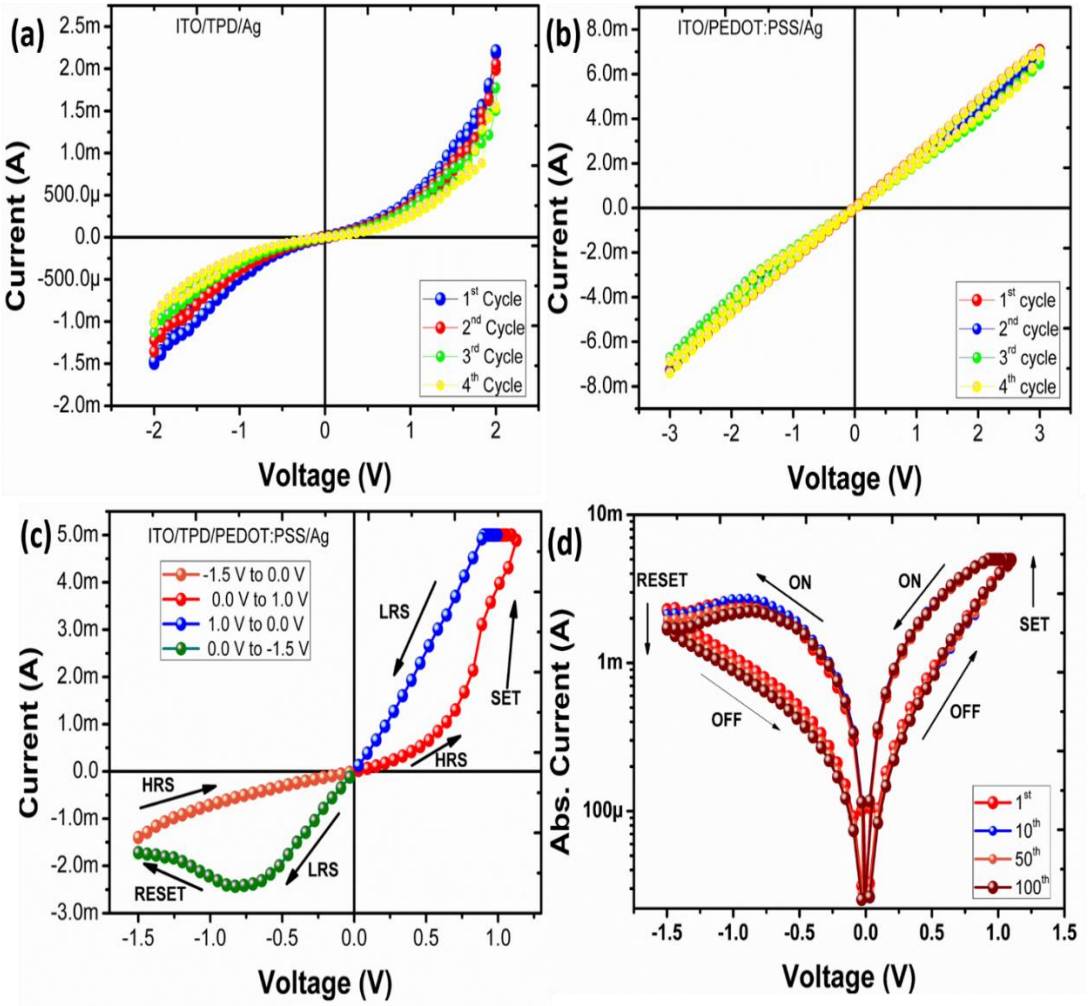

Figure 2.14 (a) I-V curve of ITO/TPD/Ag structure. (b) I-V curve of ITO/PEDOT:PSS/Ag structure.(c) I-V curve of ITO/TPD/PEDOT:PSS/Ag structure. (d) Semi-log I-V curve of the fabricated device of the ITO/TPD/PEDOT:PSS/Ag structure shows the bipolar resistive switchi

However, we demonstrated that the bilayer of the TPD and the PEDOT:PSS can achieve the resistive switching behavior. The demonstrated device was biased with -

1.5 to +1 V and +1 to -1.5 V with a current compliance of 5 mA. The positive voltage was applied to the Ag as top electrode in contact with the PEDOT:PSS film and a ground was applied to the ITO coated film as a bottom electrode in contact with the TPD film. The I-V curve and semi log graph of the absolute current and voltage (I-V) are given in Figs. 2.14(c) and 2.14(d), respectively. However, the R_{off}/R_{on} resistance ratio is ~4, which is very low. OFF and ON state detection margin between HRS (1044.57 Ω) and LRS (266.58 Ω) is also very low and its current is very high like positive voltage side is ~5 mA and negative voltage side voltage is ~3 mA as shown in Figs. 2.14(c) and 2.14(d).

The conduction mechanism of ITO/TPD/PEDOT:PSS/Ag can be explained using trap-controlled space charge limited current (TCSCLC) model and with electron flow diagram based on HOMO and LUMO of TPD and PEDOT:PSS [82] as given in Figs. 2.15(a), 2.15(b), and 2.15(c).

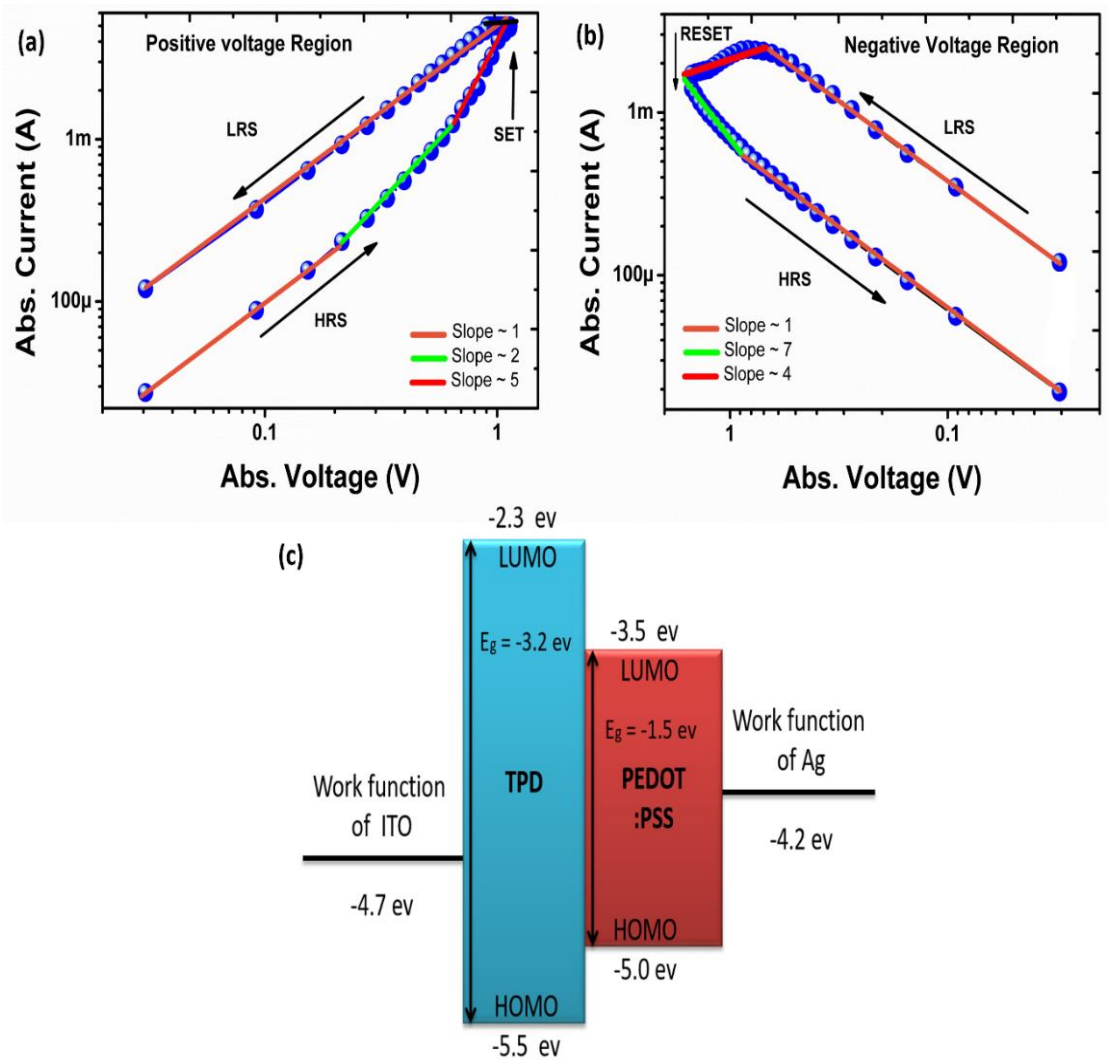

Figure 2.15 TCSCLC mechanism of ITO/TPD/PEDOT:PSS/Ag (a) positive and (b) negative voltage side. (c) Electron flow potential diagram of ITO/TPD/PEDOT:PSS/Ag structure.

However, we think the improvement of these results is required. In order to improve the R_{off}/R_{on} ratio of the memory device, we make a composite of the (PEDOT:PSS/PVOH) to increase the resistance of PEDOT:PSS with different blending ratios 3:1, 3:2, and 3:3 as shown in Figs. 2.16(a), 2.16(b), and 2.17(a). We optimized the blending ratio of the (PEDOT:PSS/PVOH) by using 3:1. Using the blending ratio 3:1, we fabricated the bilayer resistive switching device based on the TPD and the (PEDOT:PSS/PVOH) composite, and the proposed device was biased with ±1.5 V.

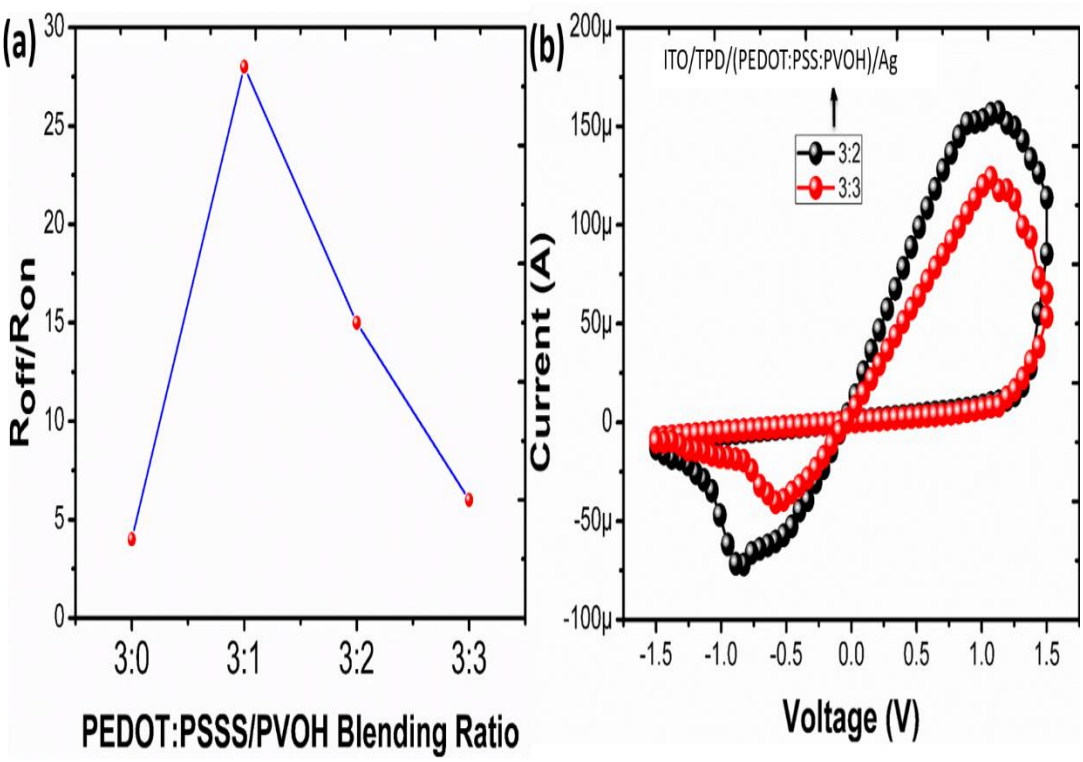

Figure 2.16 (a) Effect of Roff/Ron ratio of the PEDOT:PSS/PVOH blending ratio. (b) Resistive switching property of (PEDOT:PSS/PVOH) blending ratio (3:2 and 3:3).

Fig. 2.17(a) shows the I-V characteristics of the ITO/TPD/(PEDOT:PSS/PVOH)/Ag structure, and the current of positive and negative voltage side is decreased from 5 mA to 300 μA and 3 mA to 150 μA, respectively. The proposed memory device was initially remains in HRS from negative to positive voltage sweeping -1.5 to +1.5V, and the memory device under goes at threshold voltage +1.07 V in SET process and changes its state from HRS to LRS. During SET process, abrupt increase in current is observed. Similarly, during reverse voltage sweeping +1.5 to -1.5 V, the memory device will remain in LRS state and the memory device under goes at -1.07 V in reset process. Abrupt decrease in current is observed and the memory device shifts from LRS to HRS. As the semi-log graph of absolute I-V shown in Fig 2.17(b), the curve insures the bipolar resistive switching and the memory device is passing from origin at 0 V. As shown in Fig. 2.17(b), the memory device will remain in region 1 and 2 as an off state. It changes its state (HRS to LRS) at threshold voltage in region

3 (SET). Similarly, during reverse voltage sweep, it remains in region 4 and 5 as an on state and in region 6 and changes its state (LRS to HRS) at threshold voltage (RESET).

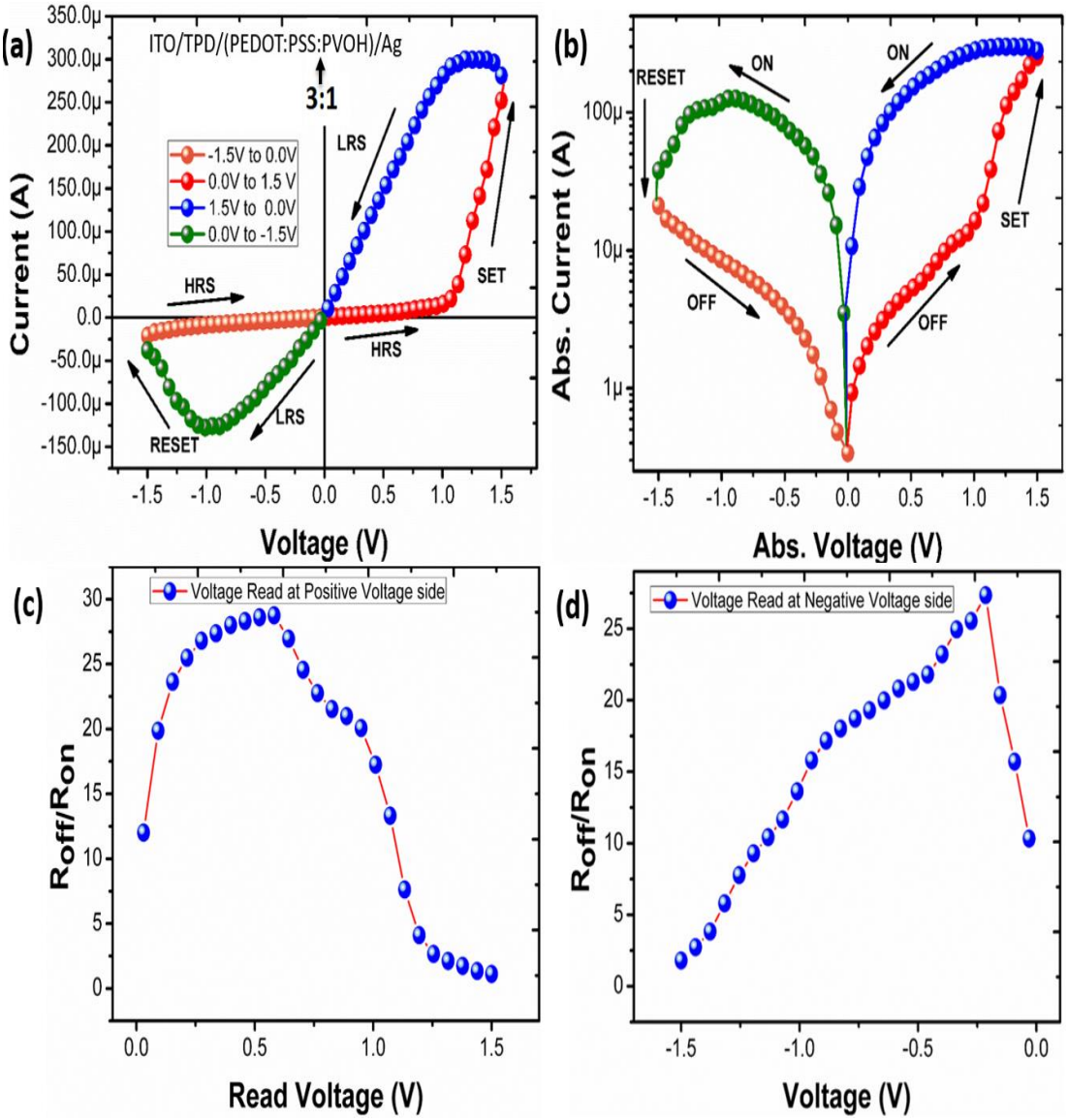

Figure 2.17 (a) I-V curve of ITO/TPD/(PEDOT:PSS/PVOH)/Ag structure, (b) Semi-log curve showing bipolar resistive switching. Read voltage of (c) positive voltage side and (d) negative voltage side.

We increased the R_{off}/R_{on} ratio of ~28.7 at a read voltage of 0.58V (positive voltage side) as shown in Fig. 2.17(c) with HRS of 97.23 kΩ and LRS of 3.38 kΩ. It is increased 7 time of the previous device (ITO/TPD/PEDOT:PSS/Ag). Fig. 2.17(d) shows the R_{off}/R_{on} ratio at negative voltage side. The forward current of LRS is

greater than the backward current of LRS, it can observed that, this function can reduce a little bit sneak current as shown in Fig. 2.17(a).

The operation reason of the proposed resistive switching device is due to the donor acceptor mechanism [83] (It is also called as a charge transaction mechanism) is occurred in between the n-type organic material PEDOT:PSS [84] composite with PVOH and the p-type organic material TPD. We can control the electron donation effect of PEDOT:PSS by making composite with PVOH, which have high band gap and insulator property and as result we can control the flow of electrons in PEDOT:PSS which have conductivity >200 S/cm and the hole mobility of TPD is ~1×10^{-4} cm^2/Vs. At the interface of TPD/(PEDOT:PSS/PVOH) free electrons in PEDOT:PSS attracts the holes from TPD and p-n junction is formed between two materials. At the interface of TPD/(PEDOT:PSS/PVOH) free electrons in PEDOT:PSS attracts the holes from TPD and p-n junction is formed between two materials. At an initial stage, the proposed device is at HRS state, and by applying voltage from -1.5 to +1.5 V, its HRS state not changes up to 0 V, but the electrons and holes move towards the p-n junction over 0 V. Operating mechanism of the device on forward bias, such that electrons flow from the Ag electrode to the ITO and donor acceptor based barrier between p-n junction decreases. The memory devices switch at threshold voltage 1.07 V and device under goes in SET process, and the device is switched from HRS to LRS. At the same stage, the electrons from Ag electrode also move into the films and support the conductive paths. During reverse bias, by applying the voltage sweep from +1.5 V to -15 V, the positive and negative charges move away from the junction, and donor acceptor based barrier between p-n junction increases and the current going to decrease and resistance is going to increase. Here, the switching of the device is changed from LRS to HRS at -

1.07 V and memory devices under goes in RESET state. That is, at -1.07 V, due to the p-n junction becomes so wide, it cannot cross the junction and the device comes to its initial stage (HRS) [85].

The conduction mechanism of an organic bilayer memory device can also be explained with help of charge tapping [86-88]. According to the charge trapping mechanism, HRS active layer have very less amount of charge carriers, which do not allow the flow of current. During positive voltage sweeping, charge carriers start trapping in an active layer at threshold voltage +1.07 V. The active layer have maximum number of trap charge carriers and the memory device shifts from HRS to LRS state as shown in Fig. 2.18(a). In order to bring back the memory device in HRS, a reverse voltage will be applied and at threshold voltage -1.07 V, the decrease in trap charge carriers and emptied at the end as shown in Fig. 2.18(b) [89].

The described mechanism is well supported with absolute current and voltage (double logarithmic) I-V graph. The HRS has three different values of slopes values, which ensures that conduction is due to the TCSCLC model. The LRS have orange marked region with slope ~1 and HRS consists of three slope regions as orange, green, and red colors marked in Figs. 2.18(a) and 2.18(b). The orange marked region has slope ~1, which indicates the ohmic conduction region, the green marked region corresponds to child's law, and the red marked region represents the state transition region (HRS to LRS) with sharp increase in current.

At a low applied voltage, the HRS shows the ohmic behavior ($I \propto V$) due to thermally generated charge carriers (orange marked region). With increase in applied voltage, trap charges also increases (the green marked region). Trap charges continuously increases with applied voltage, at threshold voltage 1.07 V, all empty traps are filled with charge carriers and exponential increase ($I \propto V^m$) in current is

observed and the memory device shifts from HRS to LRS. After this, the memory device in LRS shows the high mobility of charge carrier, where it again governs by the ohmic conduction with slope ~1 (the orange marked region).

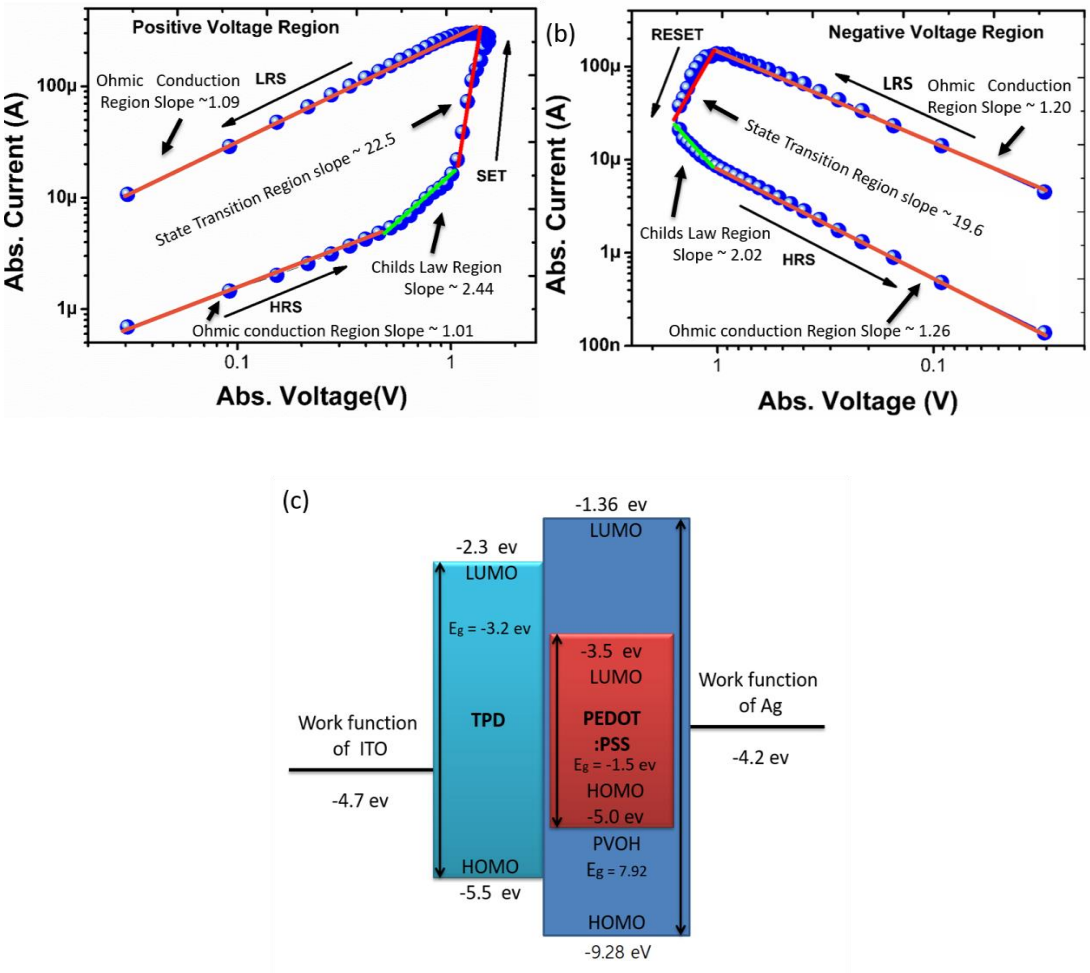

Figure 2.18 TCSCLC mechanism of the proposed memory device showing (a) positive and (b) negative voltage region, (c)The energy band diagram of organic resistive memory device showing the HOMO and LUMO of TPD and (PEDOT:PSS/PVOH) used as an active layer along ITO as

The TPD and PEDOT:PSS/PVOH can be presented in the form of potential diagram, which consist of highest occupied molecular orbit (HOMO) and lowest unoccupied molecular orbit (LUMO). Each material has different depth of potential barrier owing to different in energy level of HOMO and LUMO values of TPD, PEDOT:PSS, and PVOH. The difference in work function of each material plays an important role in creating energy barrier, which retains the electrons in their energy

state, hence we have resistive switching behavior. As shown in Fig. 2.18(c), the HOMO and LUMO values of TPD (-5.5 eV and -2.3 eV), PEDOT: PSSS (-5.0 eV and -3.5 eV), and PVOH (-928 eV and -1.36 eV) [90]. The PVOH is an insulator material and has a high band gap. Hence, it increases HRS of bilayer memory device. In order to increase the resistance of PEDOT:PSS,, we added PVOH with PEDOT:PSS. PEDOT: PSS acts as a donor and TPD act as an acceptor. The PEDOT:PSS has a lower work function of -1.5 eV as compared to the TPD -3.2 eV. Depending on the polarity of the applied voltage, electrons will move from HOMO of the TPD to HOMO of the PEDOT:PSS/PVOH or HOMO of the (PEDOT:PSS/PVOH) to HOMO of the TPD.

Fig. 2.19(a) shows the stable switching between HRS and LRS. The proposed memory device was continuously tested for more than 300 cycles as shown in insert Fig. 2.19(b). The time duration for which resistive switching device can retain its data (HRS and LRS) without any power is called retention time. The fabricated bilayer resistive switching memory device was set under observation for 10^4 sec to observe its stability in term of retention time, and the memory device has shown a stable switching as shown in Fig. 2.19(c). The organic polymers are extremely flexible and very light in weight. The mechanical robustness of the fabricated device was tested through manual control bending machine. The bending of the memory device is shown in insert Fig. 2.19(d), and tested from 50 mm to 10 mm to ensure the device stability of both HRS and LRS. The robustness of the device under bending measurement without any prominent changes in obtain result makes it an extremely useful choice for a flexible memory device.

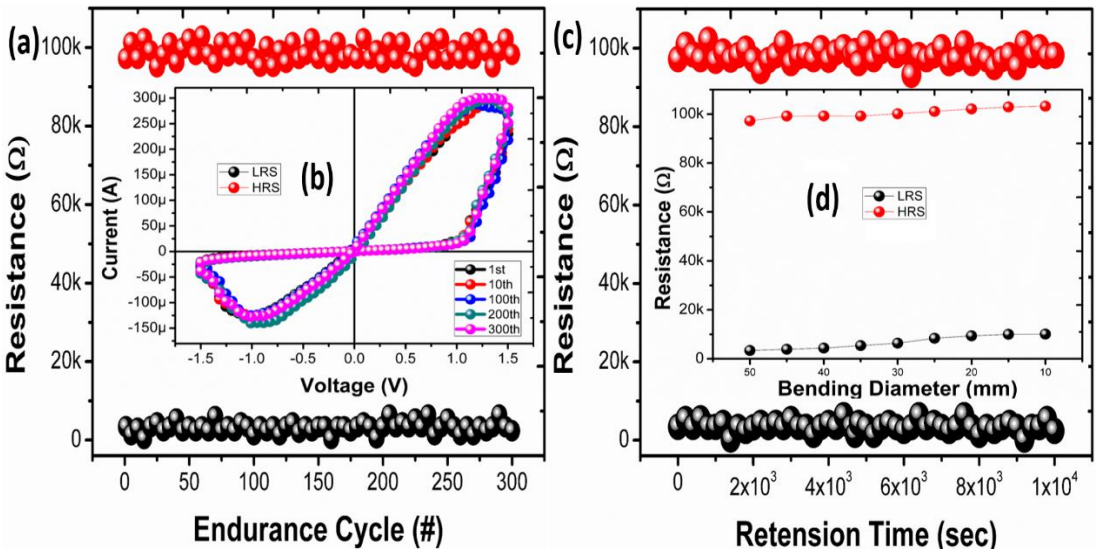

Figure 2.19 (a) The memory device with ITO/TPD/(PEDOT:PSS/PVOH)/Ag shows the stable switching function between HRS and LRS for more than 300 switching cycles. (b) The stability of the memory device for 300 cycles. (c) The retention time curve of the memory device

2.3.3 Summary

In this paper, we have proposed the novel resistive switching device based on the bilayer of the TPD and the (PEDOT:PSS/PVOH) composite, and the ITO coated PET substrate was used as a bottom electrode and Ag as a top electrode. The ITO/TPD/(PEDOT:PSS/PVOH)/Ag was operated at ± 1.5 V and HRS and LRS were recorded as, 97.23 kΩ and 3.38 kΩ, respectively. Its R_{off}/R_{on} resistance ratio shows ~28.7. The endurance of the memory is recorded more than 300 cycles and the retention time of more than 10^4 sec were tested, and the resistive memory device showed bending stability till 10 mm. The surface morphology of the fabricated device was analyzed through TESCAN MIRA 3 (STEM).The chemical and structural analysis of the active layer were also analyzed by using LabRam Horiba evolution Raman spectrometer and the elemental composition was obtained using EDS spectrometer. The mechanism of the bilayer stacked structure ITO/TPD/(PEDOT:PSS/PVOH)/Ag was explained with the charge tapping mechanism using n-type, p-type materials, and the TCSCLC model, and the electron flow potential diagram based on HOMO and LUMO of each material.

2.4 Schottky diode based resistive switching device based on ZnO/ PEDOT: PSS heterojunction to reduce sneak current problem.

The memristors is a simple passive circuit element, which memorize their internal resistance state on the basis of applied voltage [91]. Especially, a memristor is an element that links between charge and magnetic flux [92]. The theoretical concept of memristor [93] is explained by Lean Chua in 19 71, which is applicable as a transistor less switch device [94]. In 2008, Hewlett Packard (HP) group has given physical inception of a memristor fabrication [95]. After this breakthrough, it has been widely explored in numerous applications such as digital non-volatile memories [96], neuromorphic analog computation [97], and circuit applications [98].

In order to improve resistive memory performance, many researchers are exploring new materials to fabricate memory devices by using an active layer based on a single insulator such as metal oxide [99], metal sulfide [100], phase change material [101], nonmetal oxide [102] and composite materials [103] based on ion migration, redox reaction, or electrode metallization. However, to find a desired performance of a memory device, researchers are optimizing following parameters like R_{off}/R_{on} ratio, current density, switching speed, stability, and retention time [104,106]. These characteristics have strong dependency on material of electrode and active layer [107,108]. Researchers are working to enhance the performance of resistive memory device with memory structures like heterojunction of p-type and n-type materials, which have been utilized to fabricate a novel multifunctional resistive switching devices [109]. For examples, a resistive switching device with heterojunction of two materials [110] based on ion migration and defects was realized [111], and heterojunction memory devices based Pt/n- Type TiO2/p- Type NiO/Pt [112] and WO_x/AlO_y [113] have been also demonstrated.

The read current error and sneak current is required to be minimized for commercialization of resistive switching device. Due to this reason, several researchers have been exploring one diode one resistor based memory device [114] and asymmetric memory function devices [115] to control sneak current [116]. Hence, we explored a novel Schottky diode based a high charge density resistive switching device using n-type Zinc Oxide (ZnO) [117] and p-type poly(3,4ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) [118]. The Schottky diode behavior of ITO/ZnO/Ag [119] is utilized to fabricate memory function by using bilayer of n-type ZnO and p-type ZnO/PEDOTPSS heterojunction. There are different schottky diodes are investigated [120,121] in which ITO/ZnO/Ag based schottky diode is preferred due to a high forward and reverse current ratio [119]. The high electron concentration in ZnO [122] is the main reason of schottky diode behavior with ITO and the high band gap Eg ~ -3.2 eV of ZnO with HOMO -7.5 eV and LUMO of -4.3 eV [123,124], where barrier height between ITO and ZnO is -2.8 eV, which help to provide a high rectification ratio. The p-type PEDOT:PSS is a π conjugated organic polymer, which is consist of two ionomers, which has highly trnasparent. The PEDOT is based on poly thiophene and has positive charge, while PSS is based on syrene sulfonate and it carries negative charge [125]. Due to the presence of PEDOT as a p-type charge carrier [126] in PEDOT:PSS. It enhances the hole mobility, and the high band band gap difference of PEDOT:PSS with ZnO Eg ~2.3 eV helps to enhance the schottky diode function into resistive memory function.

The proposed memory device is fabricated by sandwiching the active layer based ZnO/PEDOT:PSS heterojunction between ITO coated PET as bottom electrode and Ag as top electrode through printing techniques. Here, the heterojunction layer was fabricated on ITO coated PET substrate through the spin coater and silver (Ag)

epoxy top electrodes were manually deposited. The fabricated devices were characterized for electrical properties on Agilent Semiconductor Device Analyzer (B1500A). For evaluation of mechanical properties, flexibility tests were analyzed on indigenously developed bending setup. It is also analyzed for surface morphology through field emission electron microscopy (FE-SEM), and for chemical interaction Raman spectroscopy was used. The energy dispersive X-ray spectroscopy (EDS) was analyzed to predict element composition of Ag, ZnO, and PEDOT:PSS. From these characterizations, the HRS and the LRS of proposed memory device are 531047870.8 Ω and 1001636.011 Ω, respectively at voltage read of ~1.28 V in forward current with R_{off}/R_{on} ratio is recorded as ~530. In reverse current the HRS and LRS are recorded as 153081392.6 Ω and 19034020.25 Ω, respectively at voltage read of ~ -1.28 V with R_{off}/R_{on} ratio ~8.04. From these results, we realized the resistive switching device with the asymmetric function to reduce the sneak current.

2.4.1 Materials and Methods

Flexible indium tin oxide (ITO) coated polyethylene terephthalate (PET) substrate of surface resistivity 60 Ω/sq, high-conductivity grade PEDOT:PSS with (3-4 wt.% solid content, conductivity > 200 s/cm, viscosity 10-30 cp, density 1.011 g/cm^3), 40 wt.% ZnO dispersionin ethanol (particle size < 130 nm, density 1.25 g/mL), deionized water, N,N-Dimethyl formamide (anhydrous 99.8%), Ethanol were purchased from Sigma-Aldrich(South Korea). While Ag epoxy having (specific gravity = 4) was purchased from circuitworks..For the fabrication of memory device inks were prepared as following: Intially 10 wt.% PEDOT:PSS ink was prepared by diluting PEDOT:PSS in 10 ml deionized water and40 wt.% ZnO dispersion in ethanol and both inks were placed on magnetic stirrer for 2 h at 1000 rpm and bath

sonicated by for 10 min, and centrifuged at 3000 rpm for 2 min.Before proceeding to the fabrication process: a substrate was cleaned by using isopropyl alchol (IPA) and acetone for 20 min, and then rinsed with deionized water and dried by hot air to eliminate moisture content. Surface roughness of the substrate was generated by ultraviolet (UV) treatment for 7 min. The ZnO layer was deposited by using the spin coater (EJD Tech (JSPA4)) in pulses, at 500 rpm for 9 s and 3000 rpm for 30 s, then annealed for 4 h at 120 ^{o}C. The PEDOT:PSS ink layer was also deposited by using the spin coaterin in pulses, at 500 rpm for 9 s and 3000 rpm for 30 s, then annealed for 4 h at 100 ^{0}C. Finally, the fine top electrodes of the silver (Ag) epoxy were deposited on the fabricated active film and cured at 60 ^{o}C for 30 min as shown in Fig. 2.20.

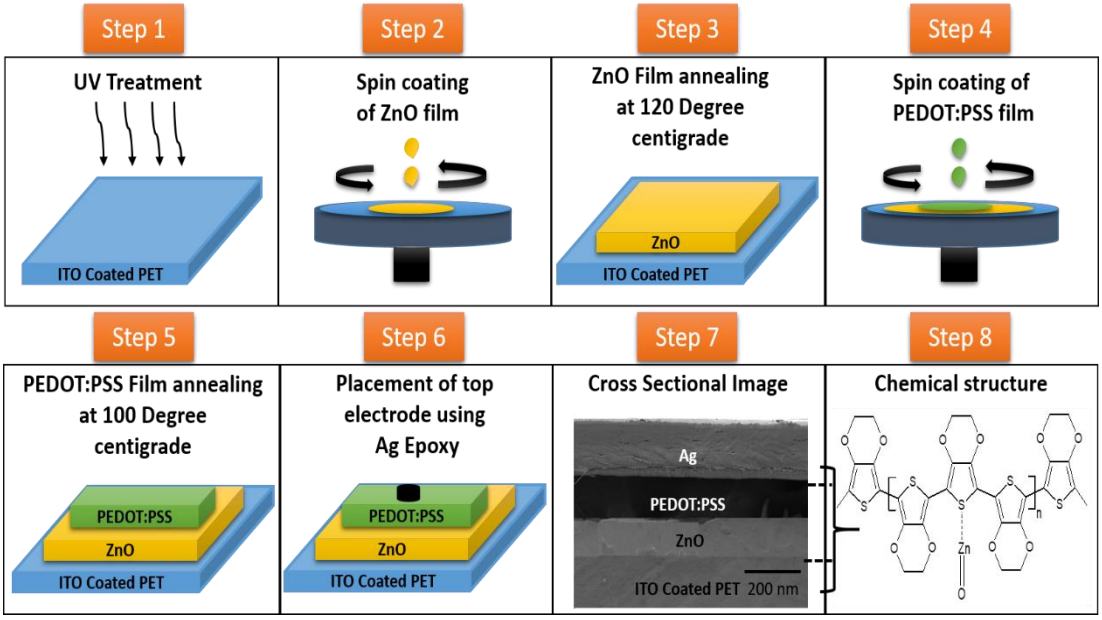

Figure 2.20 Fabrication process of the proposed ITO/ZnO/PEDOT:PSS/Ag heterojunction memory device. Here step 7 and 8 are cross sectional image of the memory device and chemical Interaction of p-type and n-type materials, respectively.

2.4.2 Characterization

Active layers surface morphology was analyzed by the field emission electron microscopy (FE-SEM Jeol JSM-7600F, Japan) at accelerating voltage of 5 kV. As

the cross sectional image shown in Fig. 2.20, the proposed device ensures that all layer are properly fabricated with the spin coater with a magnification level of 200 nm. The Surface morphology of active layer based on PEDOT:PSS is shown in Fig. 2.21a, ZnO is shown in Fig. 2.21c and Ag is shown in Fig. 2.21e with magnification of 1 um is used to analyze the EDS spot profile by using energy dispersive X-ray spectroscopy (EDS) analyzer.

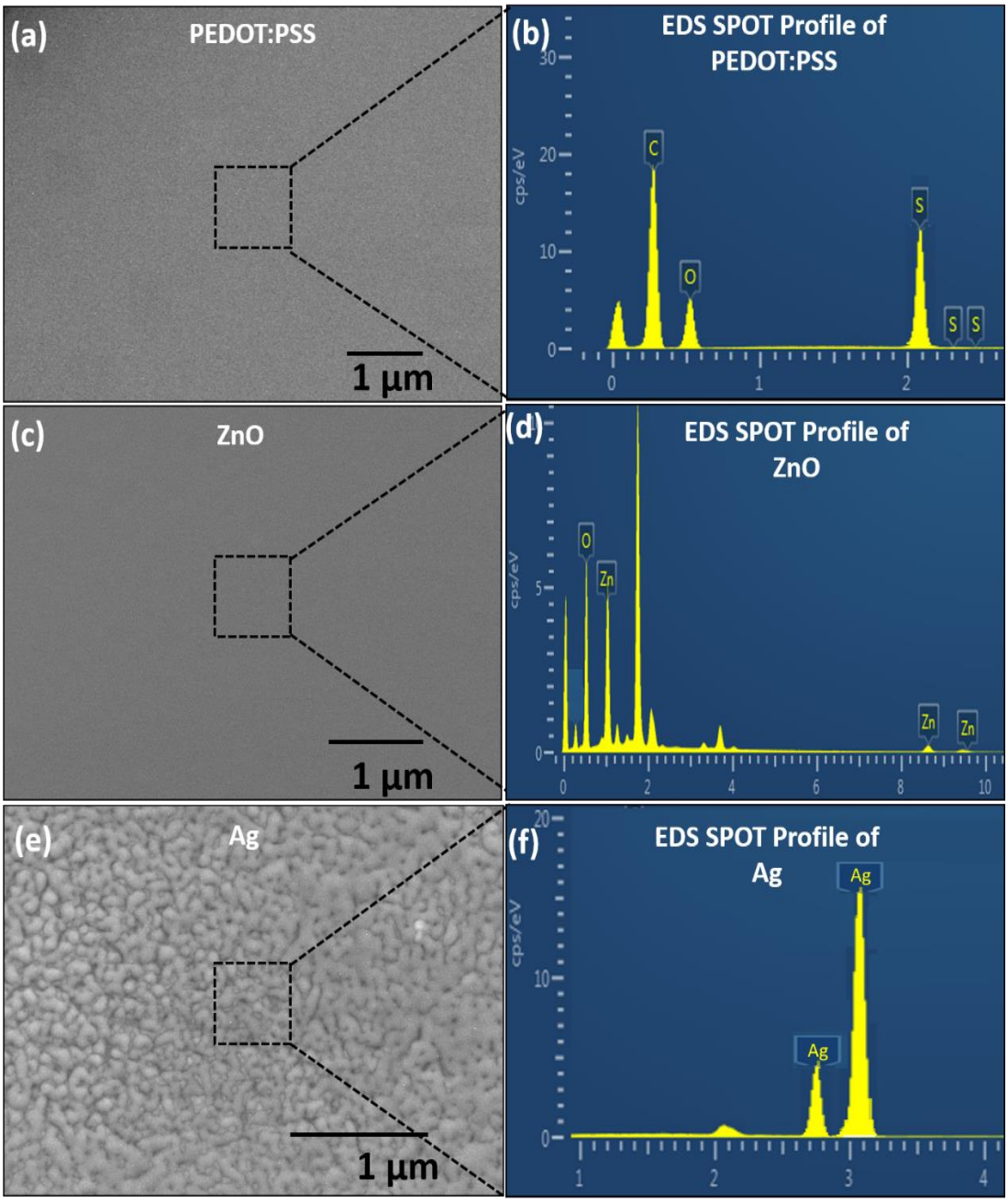

Figure 2.21 (a) SEM image of PEDOT:PSS and (b) the EDS spot profile of PEDOT:PSS, which shows the presence of C, O and S. (c) SEM image of ZnO and (d) EDS spot profile showing Zn and O peaks.(e) SEM of Ag and (f) EDS map of Ag.

The spot-profile EDS of the PEDOT:PSS, ZnO, and Ag is shown in Figs. 2.21b, 2.21d and 2.21f. The C, O, and S peaks are from PEDOT:PSS as shown in Fig. 2.21b. The Zn and O peaks are from ZnO as shown in Fig. 2.21d and the Ag peaks are from top electrodes as shown in Fig. 2.21f.The elemental composition of the ZnO and PEDOT:PSS are analyzed by the energy dispersive X-ray spectroscopy (EDS) as

depicted in Figs. 3 and 4. The SEM image shown in Fig. 2.22a with magnification of 10 μm is used to analyze the EDS mapping of the ZnO film. The EDS mapping of the ZnO shown in Fig. 2.22b, which insures the presence of the Zinc (Zn L series) in Fig. 2.22c and oxygen (O L series) in Fig. 2.22d. The SEM image of the PEDOT:PSS shown in Fig. 2.23a with magnification of 100 um is used to investigate the EDS mapping as shown in Fig. 2.23b, which ensures the presence of the carbon (C K series) in Fig. 2.23c, oxygen (O K series) in Fig. 2.23d, and Sulphur (S K series) in Fig, 2.23e.

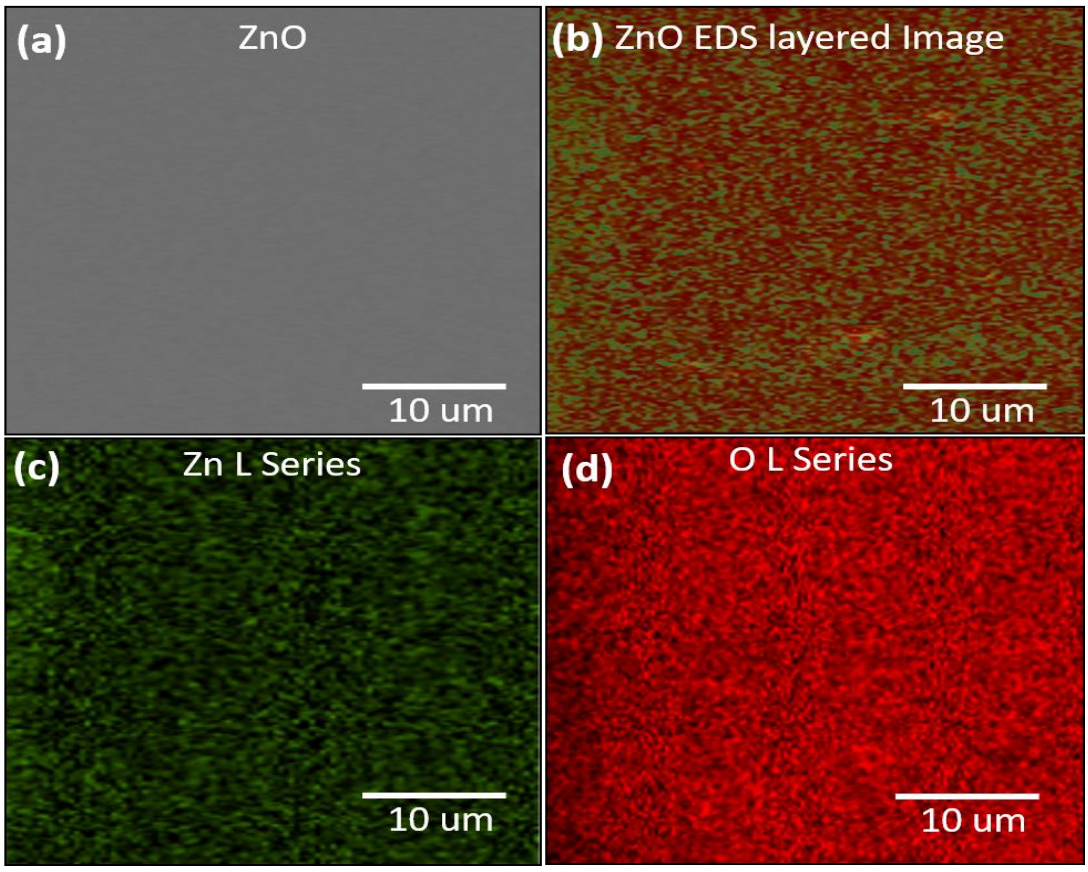

Figure 2.22 SEM of ZnO with 10 um is used to study, (b) the EDS mapping of ZnO with (c) Zn L series and (d) O L series.

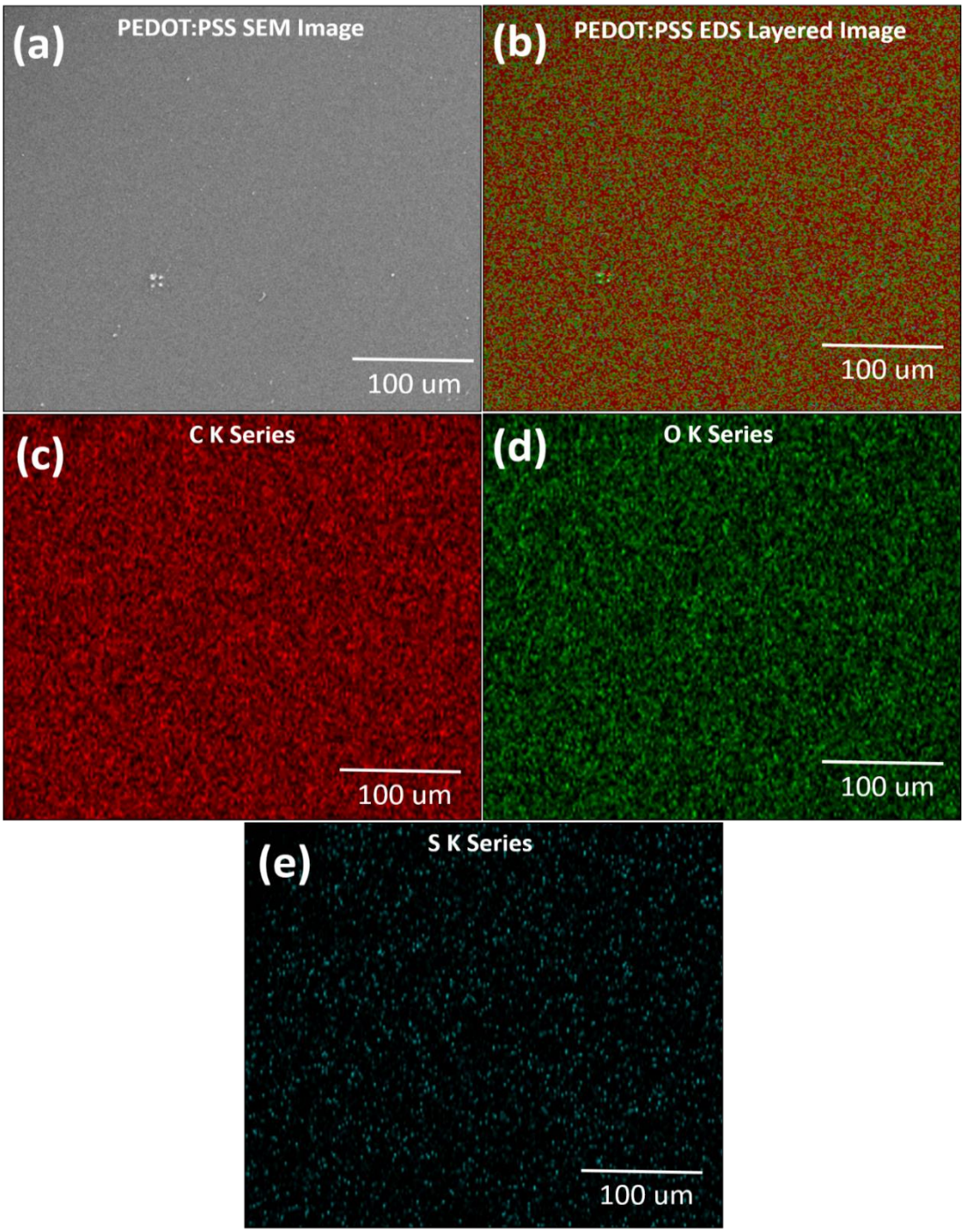

Figure 2.23 (a) SEM of the PEDOT:PSS with 100 um is used to analyze the, (b) EDS layered mapping based on, (c) C K series, (d) O K series, and (e) S K series.

Due to Raman spectroscopy is a powerful tool to characterize thin film of ZnO and PEDOT:PSS, the fabricated samples were characterized by using LabRam HR Evolution Raman spectrometer (Horiba Jobin-Yvon, France). The Raman system used an excitation source of Ar^{+} ion laser of wavelength 514 nm, which operates at a

power of 10 mW, and 10 s data-point acquisition time was employed to obtain the spectra. The Raman spectra of the ZnO and the PEDOT:PSS films are presented in Figs. 2.24a and 2.24b. In the Raman spectra of the ZnO film deposited through spin coating, there have two characteristic peaks at 99.9 cm^{-1} and 439 cm^{-1} as shown in Fig. 2.24a. The prominent peaks at 99.9 cm^{-1} and 439 cm^{-1} are attributed to $E2^{Low}$ and $E2^{High}$ phonon mode of ZnO, which corresponds to zinc atom lattice vibration and stress in the ZnO lattice, respectively. In bulk ZnO, $E2^{High}$ phonon mode observed at 434 cm^{-1}, while in the ZnO films, it is shifted at 439 cm^{-1}. The ZnO has wurtzite phase and its characteristic vibrations are due to lattice vibrations of the oxygen atoms [127]. The PEDOT:PSS Raman spectra shows a narrow prominent peak between 1400 and 1500 cm^{-1} due to characteristics of film while pristine PEDOT:PSS shows more broader band as given in Fig. 2.24b. The band at 446 cm^{-1} shows SO_2 bending, 708 cm^{-1} exhibit C-S-C deformation, 905 cm^{-1} shows oxy-ethylene ring deformation, and 1040 cm^{-1} band attribute to C-O-C deformation. The band at 1258 cm^{-1} shows Cα−Cα inter ring stretching, 1373 cm^{-1} exhibit Cβ−Cβ stretching, 1444 cm^{-1} attribute–to symmetric Cα = Cβ, 1511 cm^{-1} and 1568 cm^{-1} attribute to asymmetric Cα = Cβ stretching [128].

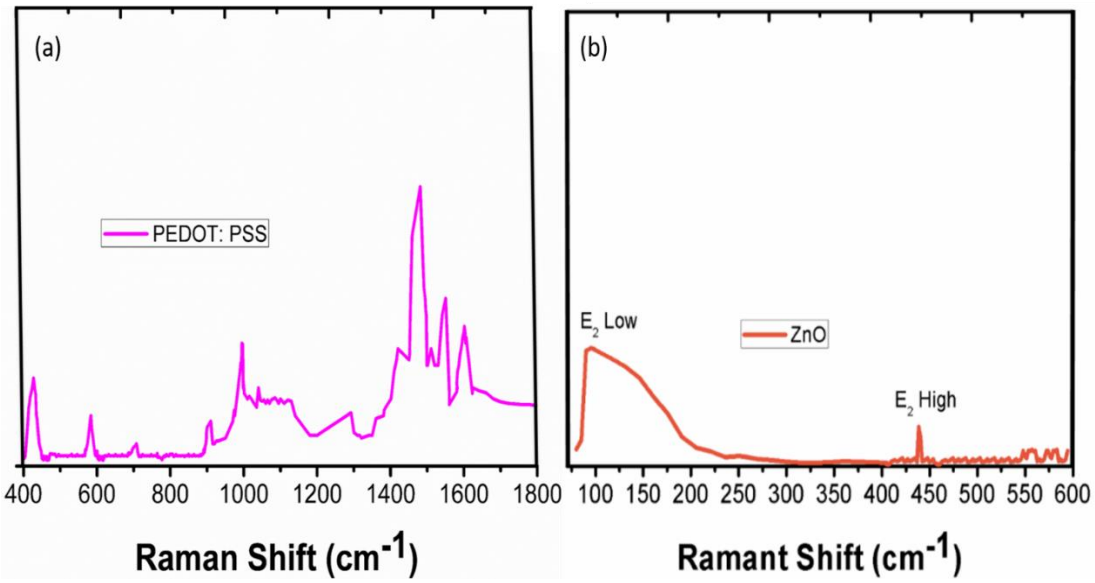

Figure 2.24 Raman shift of (a) PEDOT:PSS and (b) ZnO

2.4.3 Result and Discussion

Electrical characterizations of the proposed resistive switching device were performed by using Agilent B1500A Semiconductor Device analyzer connected with Probe Station. To characterize each material, we fabricated and analyzed single layers of each material. The fabricated devices were placed in the probe station, and the top and bottom electrodes were connected with probes. To observe the diode function in ZnO film, the dual bias voltage sweep of ±3 V was applied across the device with structure of the ITO/ZnO/Ag as shown in Fig. 2.25a. Similarly, we checked ITO/PEDOT:PSS/Ag with double sweep voltage of -3V to +3V, it shows ohmic conduction as described in Fig. 2.25b. To investigate the fabricated resistive switching device base on the heterojunction of two layers of ITO/ZnO/PEDOT:PSS/Ag as shown in Fig. 2.25c, it was biased with double voltage sweep from −3V to +3V. During positive voltage sweep from -3 to +3 V, the memory device in region 1 and 2 maintains, its HRS under 2.3 V. After the threshold voltage ~ 2.3 V, memory device changes its state from HRS to LRS in region 3 (SET). Similarly, under reverse voltage sweep from +3 to -3 V, in region 4 and 5, the

memory device remains in LRS, and the memory device shift from LRS to HRS (reset) at threshold voltage of -3 V in region 6. As the double log I-V graph as shown in Fig. 2.25d, the memory device ensures bipolar resistive switching and passes from zero volt. The R_{off}/R_{on} ratio ~530 was recorded at read voltage of 1.28 V in the forward current as shown in Fig. 2.25e, and its HRS and LRS are 531047870.8 Ω and 1001636.011 Ω, respectively at voltage read 1.28 V. Fig. 2.25f shows the resistance-voltage (R-V) graph, in reverse current the HRS and LRS are 153081392.6 Ω and 19034020.25 Ω, respectively, at -1.28 V with R_{off}/R_{on} ratio ~ 8.04 in the reverse voltage from 0 to -3 V. From these results, we are sure that it has an asymmetric function to reduce the sneak current. Which can be confirmed by R_{off}/R_{on} ratio difference at voltage read of ±1.28 V, which is (530 - 8.04) = 521.96.

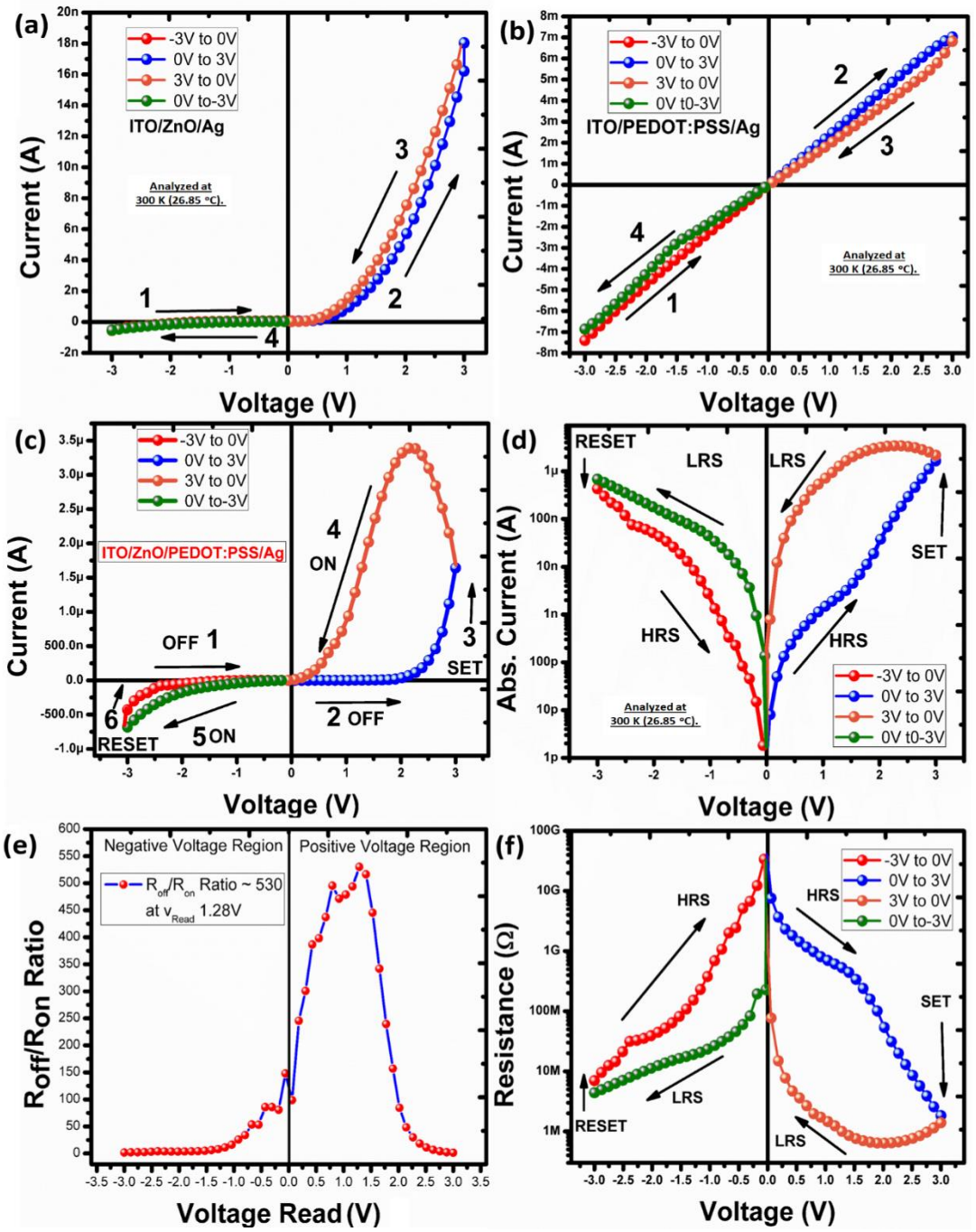

Figure 2.25 Current and voltage analysis of (a) ITO/ZnO/Ag and (b) ITO/PEDOT:PSS/Ag with biased voltage of ±3 V. (c) I-V curve of the ZnO and PEDOT:PSS heterojunction. (d) double log I-V curve. (e)The effect of Roff/Ron ratio with read voltage and (f) resistance-cu

The conduction mechanism of the heterojunction resistive memory device ITO/ZnO/PEDOT:PSS/Ag based on log-log I-V curve can be explained with the help of the charge trapping mechanism [104] as shown in Figs. 2.26a and 2.26b. The active layer during voltage sweep of -3 to +3V shows the HRS state. The main possible reason of the HRS is the presence of very less amount of a charge carrier in

an active layer. The HRS can be divided into two regions ohmic conduction region and child's law region. The ohmic conduction region ($I \propto V$) is marked with green line fitting with slope value ~1 and the amount of current flow is very less in ohmic region. In child's law region, the number of the charge carriers starts increasing with applied voltage, and it is marked with orange marked fitting with slope value ~3. At threshold voltage 2.2 V, abrupt current increasing is observed and memory device shift from HRS to LRS. This region is also known as the state transition region (red marked region: $I \propto V^n$) as shown in Figs. 2.26a and 2.26b. After this conduction filament is formed between top and bottom electrodes, the memory device under goes in LRS, during voltage sweep from +3 to -3 V and a high amount of current flow ~3.4 μA, where the resistive switching memory device again governs by an ohmic conduction ($I \propto V$) as shown in Figs. 2.26a and 2.26b. At negative threshold voltage, the memory device again has very less amount of charge carriers and its filament going to vanish and memory device shift from LRS to HRS.

As shown in Fig. 2.26c, a positive voltage is applied to Ag top electrode and a negative voltage is applied to ITO coated PET as bottom electrode. The increase in the applied voltage, there result in increase of Ag+ ion at Ag as top electrode intact with PEDOT:PSS film and the repulsion force between Ag^+ ion start increases, where PEDOT:PSS also have electron donation effect due to conductive nature of PEDOT:PSSS [129]. On the other hand, the ZnO film is in contact with ITO coated PET, where the O^{2-} ion increases with increase in applied voltage. At threshold voltage, the oxygen vacancies move upward near to PEDOT:PSS film and Ag^+ ion moves towards ZnO film. At the junction between ZnO and PEDOT:PSS, Ag^+ ion uses oxygen vacancies as a trap charges and make a filament between top and bottom electrode and memory device moves from HRS to LRS and the memory devices

under goes in SET process and abrupt increase in current is observed. In order to back the resistive memory device in HRS, a reverse voltage sweep is applied to top and bottom electrodes as shown in Fig. 2.26d. After this, Ag+ start moving upward and oxygen O^{2-} vacancies move downward, and the filament will going to decrease at negative threshold voltage, it will break and the amount of the current will decrease, and the memory device under goes in HRS (RESET) as shown in Fig. 2.26d.

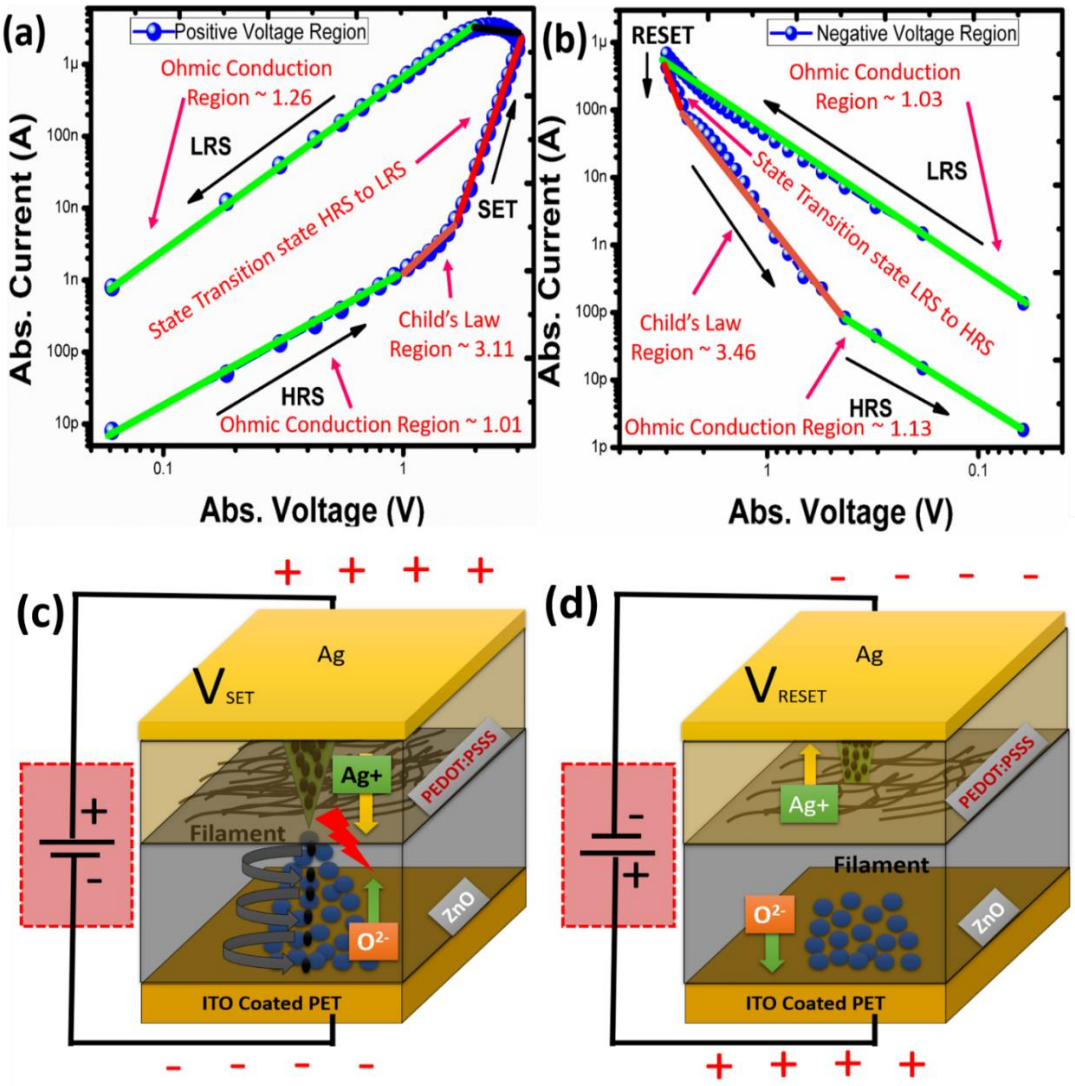

Figure 2.26 TCSCLC mechanism of the proposed hero junction memory device (a) positive voltage region and (b) negative voltage region. Ag ions migration mechanism showing (c) set and (d) reset process

To demonstrate the proposed schottky diode base resistive switching, we used a p-type PEDOT:PSS and a n-type ZnO as shown in Fig. 2.27a. At the ZnO-PEDOT:PSS

interface, free electrons from the ZnO diffuse into PEDOT:PSS layer, and holes from PEDOT:PSS begin to diffuse into the ZnO layer. The holes and electrons form an interface charge depletion region, and a p-n junction is formed as described in Fig. 2.27a. The I-V characteristics of the proposed device are also described the p-n junction asymmetric resistive switching behavior based on schottky diode. Initially, the memory device is in HRS state, and by applying voltage sweep from -3 to +3V. Over zero volt p-n junction barrier between PEDOT:PSS and ZnO will decrease, and the device will shift from HRS to LRS (SET) due to a high amount of the current flow. At the same stage, Ag+ ions migrate into the active layer and support the current flow. The interface of ZnO/PEDOT:PSS is expected to exhibit the rectification characteristics because of their p-type and n-type material nature [130]. In contrast, for an asymmetric bipolar device [115], the switching polarity is often governed by the asymmetry of the device stack rather than the polarity of electroforming [131]. During the reverse voltage sweep +3 to -3V, the p-n junction based on donor acceptor going to increase, very small amount current will going to flow, and the resistance going to increase, due to p-n junction becomes so wide up to no more charges can flow through the active layer. Here, the memory device comes back to its initial stage HRS at threshold voltage.

The PEDOT:PSS and ZnO can be presented in the form of the highest occupied molecular orbit (HOMO) and the lowest unoccupied molecular orbit (LUMO) as shown in Fig. 2.27b. The PEDOT:PSS and ZnO have different depth of the potential barrier, with different in depth between HOMO and LUMO. The difference in work function of PEDOT:PSS and ZnO plays an important role to retain electron in an energy state, and as a result, we are sure that it has the schottky diode base resistive switching behavior. As shown in Fig. 2.27b, the HOMO and LUMO values of

PEDOT:PSS (− 5.0 eV and − 3.5 eV) , and ZnO (-7.5 eV and -4.3 eV). The HOMO to HOMO difference of PEDOT:PSS and ZnO is 2.3 eV and LUMO to LUMO is 0.8eV. From energy band gap diagram, we can easily say that, electrons need more electric field to move from HOMO to HOMO. Hence, PEDOT:PSS acts as acceptor and ZnO acts as donor. The PEDOT:PSS has a lower work function of -1.5 eV as compared to the ZnO -3.2 eV. Depending on the polarity of the voltage sweep, electrons will move from HOMO of the ZnO to HOMO of the PEDOT:PSS or HOMO of the PEDOT:PSS to HOMO of the ZnO, so it has the resistive switching behavior.

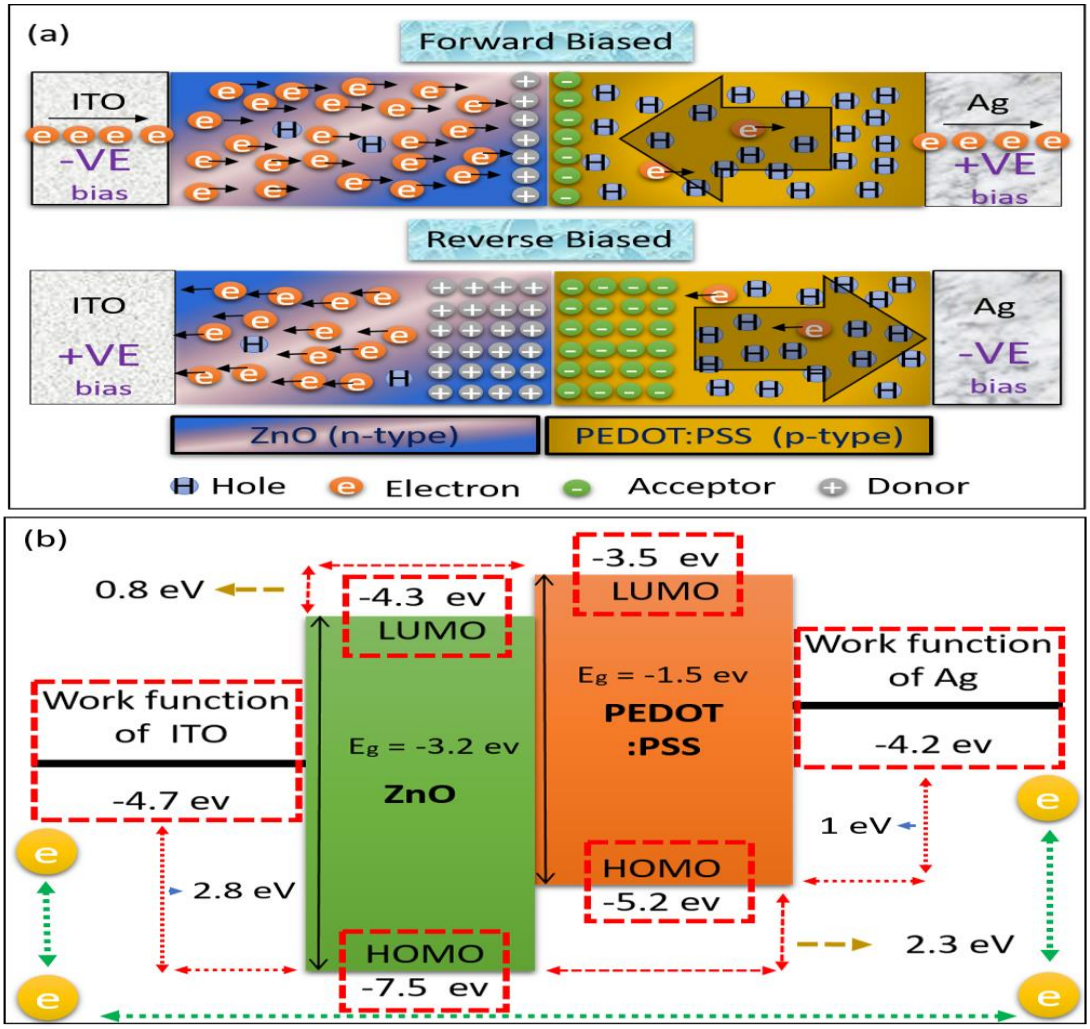

Figure 2.27 (a) Schematic illustration of the schottky diode base memristor with p-n-heterojunction. (b) Operating principle of the device using energy band diagram.

The ITO/ZnO/PEDOT:PSS/Ag memory device is continuously tested for more than 500 endurance cycles as shown in Fig. 2.28a, and it shows a stable memristor function with invariable change in the resistance states as shown in Fig. 2.28b. The states are retentively analyzed after device encapsulation with PDMS for more than 30 days as shown in Fig. 2.28c and we observed the stable memory functions as shown in Fig. 2.28d. The retention time and the endurance cycle stability tests were analyzed at room temperature 26.85 ^{o}C.

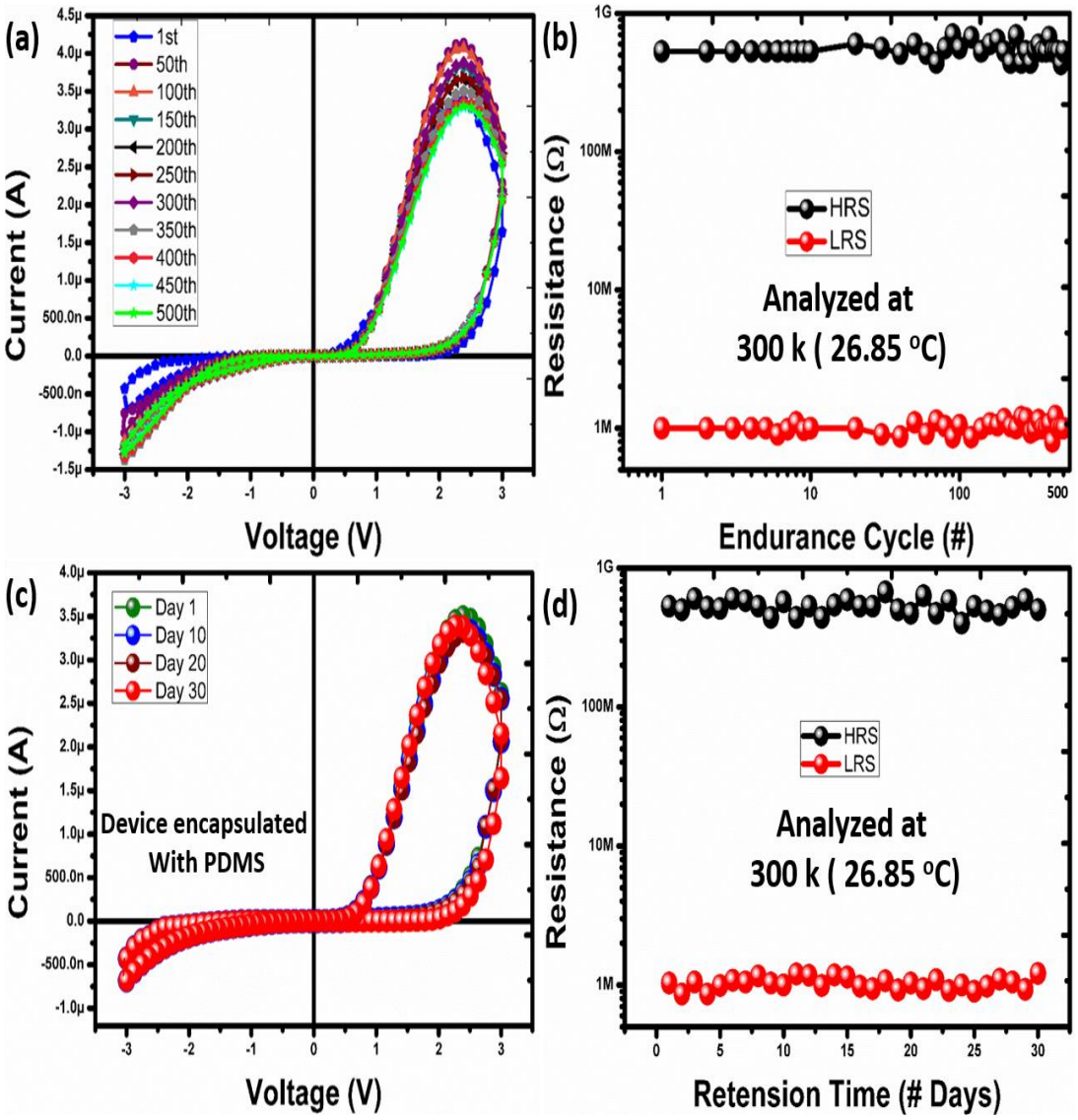

Figure 2.28 (a) HRS and LRS state of the resistive switch for 500 endurance cycles. (b) Endurance stability of the proposed device of for more than 500 cycles. (c) Retention time of the proposed device. (d) Retention stability of the memory device.

The mechanical properties were evaluated by bending it on different diameters from flat down to 4 mm diameter by utilizing indigenously made bending setup as shown in Figs.2.29a and 2.29b. Minimum bending diameter was found 10 mm, and beyond it, due to the deterioration of the active layer device behaved open circuited as shown in Fig. 2.29c.

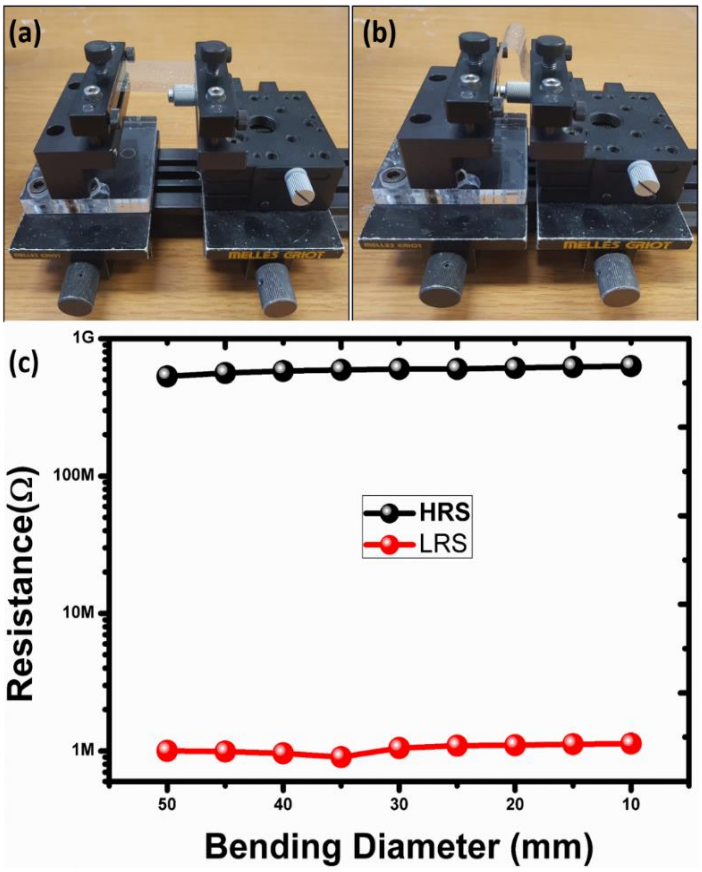

Figure 2.29 The mechanical testing setup (a) on flat surface and (b) 4 mm diameter. (c) Bending test results from 50 mm to 4 mm.

2.4.4 Summary

By using the printed technique, we proposed the schottky diode base high charge density resistive memory device based on ZnO/PEDOT:PSS heterojunction on ITO coated PET substrate, and its top electrode was deposited by Ag epoxy. The ZnO/PEDOT:PSS heterojunction layers were fabricated through the spin coater. The surface morphological characterizations were examined by FE-SEM, and elucidated

uniformly deposition of layers. The device showed schottky diode based resistive switching across voltage of ±3 V. For the forward current, the HRS and LRS were found as 531047870.8 Ω and 1001636.011 Ω, respectively, and its R_{off}/R_{on} is 530. To block the sneak current, HRS and LRS were measured at ~ 1.28V as 531047870.8 Ω and 1001636.011 Ω, respectively in the reverse current with R_{off}/R_{on} ratio ~8.04 and we checked the R_{off}/R_{on} ratio difference in Forward and reverse current (530 - 8.04) = 521.96, which ensures the device decreases the sneak current problem in cross bar array. The 500 endurance cycles and the retention time of 30 days were tested, and it showed a very stable memory performance. In flexibility test, it exhibited down to 10 mm diameter, and the device got open circuit beyond 10 mm. The chemical investigation was analyzed using Raman spectroscopy, and the element analyses were performed with the energy dispersive X-ray spectroscopy (EDS). The proposed device can open a new gate way for stable and flexible memory devices for a high dense crossbar array to reduce the sneak current.

Chapter 3 Conclusions and Future Work

This chapter presents the overall conclusions of the thesis dissertation and highlights the contribution made in the solution processed printed and flexible electronics fields.

3.1 Overview and General Conclusions

Solution processed printed electronics is a new technology that enables flexible, wearable, stretchable, low cost and large area devices. These printed electronic devices are emerging in the present electronics industry to cover the cost and technological gaps associated with conventional electronic processing and application demands. So the demands of low cost, targeted applications, flexibility, and low temperature processing forcing the research and industry to work on this new emerging branch of electronics.

Solution processed Printed electronics is quite new field, hence facing many problems include fabrication techniques, printable materials for device and as well as for encapsulation of the manufactured devices to make them reliable for long life time. In past two decades, huge efforts have been made in processing of organic and inorganic materials to make them printable for printed electronics. Apart from the material exploration and processing for the new devices, fabrication techniques are also under research to enable them for efficient fabrication. Some fabrication techniques are developed and been adopted by the solution processed electronic industry such as inkjet, spin coater and EHD, however some techniques are under study yet. In this thesis work spin coater and Inkjet printer are used for the fabrication of devices. Materials including organic and inorganic are synthesized and processed for the low-cost fabrication techniques, and their deposition is confirmed

with characterizations. This thesis contributes to the Research and Development R&D community to address the challenges in the fabrication process of solution processed all-printed electronic devices and circuits. Main contributions are listed as below:

Resistive memory devices can play an important role in the future for data storage. We propose a stable non-volatile resistive switching based on nano-composite of inorganic and organic materials, Zirconium dioxide (ZrO_2) and Poly (4-vinylphenol) (PVP), respectively. The active layer of ZrO_2: PVP composite is fabricated by using spin coater on indium tin oxide (ITO) coated Polyethylene terephthalate (PET) substrate, and the top electrodes are patterned by using silver (Ag) epoxy. The resistive random access memory (RRAM) demonstrates a bipolar resistive switching at low operating voltage of ±1.5 V. The high resistance state (HRS) and low resistance state (LRS) are 11.44 kΩ and 262.25 Ω, respectively, and the obtained R_{off}/R_{on} resistance ratio is ~ 44.

Device stability is very import feature. In this expect, we propose a novel bilayer resistive switching device based on N,N′-Bis (3-methylphenyl)-N,N′-diphenylbenzidine (TPD) and Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate)/ Poly(vinyl alcohol) (PEDOT:PSS/PVOH) composite. The bilayer structure of TPD and (PEDOT:PSS/PVOH) is fabricated on indium tin oxide (ITO) coated Polyethylene terephthalate (PET) substrate through all printed technology. Here, the ITO acts as a bottom electrode and the top electrode is patterned by using silver (Ag) epoxy. The fabricated device has a high resistance state (HRS) of 97.23 kΩ and a low resistance state (LRS) of 3.38 kΩ at read voltage of 0.58 V, which is achieved R_{off}/R_{on} resistance ratio of ~28.7. The proposed device maintained its stability for more than 300 endurance cycles and retention time of

more than 10^4 sec.

To realize an asymmetric function and to block sneak currents in memory device, we propose a novel schottky diode based high charge density resistive switching device based on zinc oxide (ZnO) and poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) heterojunction, which is structured with bottom and top electrode as indium tin oxide (ITO) and silver (Ag), respectively. The heterojunction layers are deposited through a spin coater on ITO coated polyethylene terephthalate (PET) substrate. The hetrojunction resistive switching device is measured over more than 500 endurance cycles on dual polarity voltage of ±3 V. The stability of the memory device is analyzed for more than 30 days with high resistance state (HRS) and low resistance state (LRS) as 531047870.8 Ω and 1001636.011 Ω, respectively, at reading voltage of 1.28V in forward current, and its R_{off}/R_{on} ratio is recorded as ~530. In reverse current, the HRS ~ 153081392.6 Ω and LRS ~19034020.25 Ω are recorded at voltage read of ~ -1.28 V, with R_{off}/R_{on} ratio ~8.04, which insure that memory device help to reduce the sneak current. Hence, the proposed resistive memory devices can be applied in flexible resistive switching devices to blocking sneak current problem.

3.2 Future Work

Every device can be improved by mean of fabrication technique, fabrication process or by changing material. In future, these devices can be investigated for better performance and reliability. Memory devices presented in this work with different materials can be improved for high retention time, endurance and off/on ratio. Apart from the performance improvement, integration with the exiting CMOS technology is still an issue for real time printed electronics applications. Conventional CMOS

technology is based on three-terminal transistor while the resistive switch is two-terminal device that needs different circuit design strategy.

Annex-A Journal Papers

1. **Muhammad Umair Khan**, Gul Hassan, Muhammad Asim Raza and Jinho Bae: Bipolar resistive switching device based on N, N′ -bis(3-methylphenyl)-N, N′ -diphenylbenzidine and poly(3,4-ethylenedioxythiophene): poly (styrene sulfonate)/poly (vinyl alcohol) bilayer stacked structure; October 2018 Applied Physics A 124(10) DOI: 10.1007/s00339-018-2142-z (IF: 1.694)
2. **Muhammad Umair Khan**, Gul Hassan and Jinho Bae: Non-volatile resistive switching based on zirconium dioxide: poly (4-vinylphenol) nano-composite; (Micro Electronics Engineering) (IF: 2.1) (under review)
3. **Muhammad Umair Khan**, Gul Hassan, Muhammad Asim Raza and Jinho Bae: Schottky diode based resistive switching device based on ZnO/PEDOT:PSS heterojunction to reduce sneak current problem; (Organic Electronics) (IF: 3.6) (Under review)
4. Gul Hassan, **Muhammad Umair Khan**, Jinho Bae: Stable and flexible non-volatile resistive switching device based on F8BT: PVP nanocomposite and its conduction mechanism; (Applied Physics A) (IF: 1.694) (under review)
5. Gul Hassan, Jinho Bae, **Muhammad Umair Khan** and Shawkat Ali, Resistive Switching Device Based on Water and Zinc Oxide Heterojunction for Soft Memory Applications; (Material Science and Engineering B) (IF: 3.31) (under review)
6. **Muhammad Umair Khan**, Gul Hassan and Jinho Bae: Bio-compatible and bio-degradable organic humidity sensor based on natural inner egg shell membrane with multilayer crosslinked fiber structure; (Scientific Report) (IF: 4.122) (Under review)
7. **Muhammad Umair Khan**, Gul Hassan and Jinho Bae: All Range inkjet Printed Linear humidity Sensor using 3x3 sensing array with different electrode spacing and particle size utilizing methylene blue and graphene composite. (Under progress)
8. **Muhammad Umair Khan**, Gul Hassan and Jinho Bae: Bio-compatible and Bio-degradable organic humidity sensor using Egg Albumin for environment monitoring. (Under progress)
9. Muhammad Umair Khan, Gul Hassan and Jinho Bae: Self powered humidity sensor using natural inner egg shell membrane. (Under progress)

10. **Muhammad Umair Khan**, Gul Hassan and Jinho Bae: Light controlled resistive memory device based on methylene blue and ZnO heterojunction. (Under progress)
11. **Muhammad Umair Khan**, Gul Hassan, Muhammad Asim Raza and Jinho Bae: Triboelectric Nanogenerator based on Cellelose acetate and PDMS composite. (under progress)

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